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REPRESENTATION OF EDGE LOCATION DETECTOR ON PLIC OF COMPANY XILINX

Hardware representation of edge location detector is presented in the article. The offered parallel conveyer algorithm of image processing in which, the parallel-recursive processing of data using Gauss filters with different degrees of blur is executed at the first stage. At the second stage the conveyer processing of data which make part of "sliding window" is executed. For realization of such device, the PLIC Khs3s1000 family of Spartan-3 of company Xilinx is selected.Circuit synthesis was executed in CADD of Xilinx Project Navigator 7.1, modeling was executed by means of the simulation program f ModelSim SE PLUS 5.1. Such realization of device allowed to improve the detector operation rate 20-25 times.

Keywords: *image preprocessing, rolling, pixel, low frequency filter, programmable logical integrated circuit*

Introduction. Linear processing operation, with a "sliding window" is the basis for many procedures of images processing, the essence of the operation is that some limited two-dimensional area, "window of processing", consistently occupies all possible positions in image plane. The value of one initial image indication is calculated for every window position using its indication values, which are within this window [1].

Spatially-invariant processing of such type is described by general relation [2]:

$$g(n,m) = G[\{f(n-k,m-l)\},(n,m) \in D], \quad (1)$$

where $f(n,m)$, $g(n,m)$ - two-dimensional sequence of indications of input and output images accordingly; G –change operator; D – finite set of indications plural, which defines the processing window dimensionality.

It means that the discrete image signal value at the system output is the result of digital convolution of input discrete signal with finite- pulse characteristic - FIR-filter. However, such convolution calculation has practical value only for small dimensionalities of window and small images, since calculation volume is proportional to the dimensionality of the window and image .

Prior information sources analysis. Many rapid convolution algorithms for FIR-filters are known nowadays, but because of data processing complexity, it is hardly possible to process the image rapidly, using them. Another approach aimed at processing speed increasing is the hardware realization of digital filters , which requires application of complex devices and large hardware resources. In this case, the most effective version of hardware realization is usage of programmable logical integrated circuits (PLIC).

PLIC become the most widely spread element base for using in digital signals processing (DSP). Due to developed architecture, high clock rate and low price, PLIC are irreplaceable for prototyping and short-run production.

There exists some architectures
of digital FIR-filters on PLIC: parallel, serial and serial-parallel. Digital filters with parallel architecture have the best performance and minimum delay, but require a lot of logical resources of the microcircuit. Serial filters have the least performance and maximal delay, but they are more compact, as compared with devices having parallel architecture [3].

In [4, 5] the method of refined edge detection is offered, based on the finding of intersections of common points between the filtered images due to application of low-frequency Gauss FIR-filters with different blur level , which can be described by the expression:

$$J(x,y) = p(H^*(n,m)\big|_{\sigma 1} - H^{**}(n,m)\big|_{\sigma 2}), \quad (2)$$

where $H^*(n,m)$, $H^{**}(n,m)$ – images, resulted from the low-frequency filtration with the appropriate blur levels of $\sigma 1$ і $\sigma 2$; p – scaling index.

Refined edge can be obtained, using the elementwise conversion :

$$h(n,m)=\begin{cases}1,\ if\quad J(n-1),m)\cdot J((n),m)<0;\\ 1,\ if\quad J(n-1),m)\cdot J((n),m)=0\big|_{J((n-1),m)\neq J((nm).}\\ 0,\ if\quad J(n-1),m)\cdot J((n),m)\geq 0.\end{cases}; \tag{3}$$

Since the basic processing labour-consumption of such method is concentrated in the arithmetic convolution operations, and two convolution operations are used in this method, then processing time grows practically twice.

The goal of research is to increase processing speed of edge detector, based on the low-frequency PLIC-based Gauss filter.

Materials and results of investigations. The parallel conveyer algorithm of preliminary image processing, according to which the parallel-recursive data processing with low-frequency Gauss filters with different blur levels is executed at the first step. At the second step, the elementwise subtraction operation of two filtered images are executed.

The flow diagram of such processing is showed in Figure 1. Such detector has input/output devices, two buffer storages (MS1, MS2), which provide continuous information recording and read-out, two Gauss filters (GF), and also elementwise subtraction arithmetic operations device (Sub).

In Figure 2 the filter flow diagram is shown, which assumes the performance of five arithmetic operations over each pixel. Such filter consists of multiplexing devices (MD), elementwise addition devices (ADD) and registers (Rg), for storage of input data of the pixel which is processed, and data of processing results.

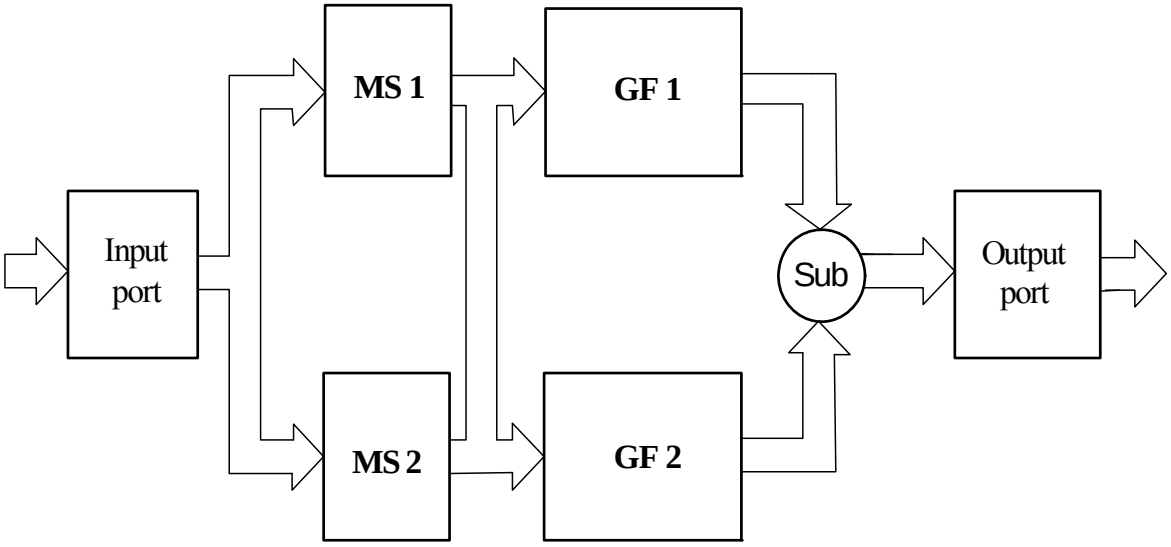

Figure 1. Structural diagram of the edge detector device

As such processing is executed over the data of all pixels, according to (1), that make part of "sliding window", then for fast-acting increase, it is suggested to use some one-dimensional filters sets, which operation is synchronized in time. The Gauss one-dimensional filter from the indications consequence of input f(n) signal, with the window width size into output sequence g(n) and is described by the relation:

$$g(n)=\sum_{l=-L^-}^{L^+}h(l)f(n-l), \tag{4}$$

where $h(l)$ – pulse characteristic of the filter , which equals zero over the limitss of the

$[-L^-,\ L^+]$ interval.

Such processing scheme provides the data read-out of every pixel, included in the processing window, with clock rate, and can be presented as a sum of K pixels values of «sliding window».

$$h(l) = \sum_{k=0}^{K-1} a_k h_k(l), \tag{5}$$

$$y(n) = \sum_{k=0}^{K-1} a_k h_k(n), \tag{6}$$

$$y_k(n) = \sum_{l=-L^-}^{L^+} h_k(l) f(n-l), \tag{7}$$

where a_k – indexes; $h_k(l)$ – linearly independent basis functions, decomposed in the numerical series; $y_k(n)$ – processing signals.

Hence, on every clock rate signal, multiplexing of these pixels on the appropriate mask coefficients is performed in pipeline manner, in every multiplexing cycle, the addition of result with previous result

is carried out. This process is executed until the end of data processing of all the pixels within the “sliding window”.

Values of pixel intensity as a rule are 24-bit by 8 bits on every color of RGB system. It means that three identical one-dimensional filters, operating parallel in time can be used for filtering.

Hardware representation of parallell conveyer processing, performed by the edge detector was realized on Xilinx company PLIC of Spartan-3 families.

The attractive feature Xilinx company PLIC for DSP algorithms realization, as compared with other manufactures PLIC is internal fast-acting distributed RAM, which is arranged in the blocks of necessary size. The use of such RAM is very effective for DSP algorithms realization by means of distributed arithmetic method, and also for coefficients storage, results of intermediate calculations, etc. Thus, due to hardware facilities to provide parallel processing operation, flexible device structure adaptation for necessary algorithm, high integration efficiency of development facilities, simple construction of highly productive DSP system becomes possible on a single crystal in the shortest possible time[6].

For realization of the above-mentioned device the PLIC Xc3s1000 families of Spartan-3of Xilinx corp. is chosen, the basic characteristics are given in the Table:

Table

Parameters of PLIC Xc3s1000 families of Spartan-3of Xilinx Corp.

System gate	Logical cells	Distributed memory, Kbits	Available input/output contacts	Maximal system frequency MHz
10^6	17 280	102 10^3	391	326

Based on the analysis given in Table 1, we can make a conclusion: PLIS Xc3s1000 families of Spartan-3 satisfies all the characteristics for detector construction.

Device description at the register transmissions level was executed on VHDL language, for obtaining of PLIS geometry file, the SAPR of Xilinx Project Navigator 7.1 is used, the filter operating imitation is executed, using simulation program - ModelSim SE PLUS 5.1.

In Figure. 3 the flow diagram of device with one one-dimensional filter is shown, this filter provides 8-bit data processing by “sliding window”, with dimensionality of 5x5.

The dual-port memory principle is used for continuous data processing implementation. After the recording of 2 KB data in RAM **mem0 the** next data is recorded in analogical memory **mem1**. That

is, while the first data portion is read from **mem0** and processed, the second portion is recorded from the port into **mem1**.

Input data is recorded by addresses which are set by the 12-digit counter **count12**. The data recording address bus is multiplexed by the multiplexer **mux22x2** with the data read address bus. After 2047 value is achieved, the signal **count(11)** is formed, which switches the multiplexer **mux22x2** into data address reading mode, multiplexer **mux_8** into data reading from memory **mem0** and **mem1** mode and starts the counter by 25 module **count_mod25**. The values **of count_mod25** are transmitted to the input of data storage (CDS) **addr_conv**, at the output of which the reading data address is formed by certain "sliding window" principle. After the counter overflow **count_mod25** the **OVF** signal is formed, which initializes the counter on the 2022 module **count2022_mod**. The result of counting is added to the result at the output (CDS) of **addr_conv**, that allows data read executing, by the addresses of new "sliding window". Thus, the data read address through the multiplexer passes to RAM address bus. The data multiplexing operation is executed in mult by the appropriate mask coefficient, which are received from CDS **coef_conv** by the counter addressing results **count_mod25**.

Each 25 cycles the results of multiplication are added, as in this case 5x5 mask is used. After addition in **sum_ 16** the division operation by the total weight coefficient of "sliding window" is executed in **div256**, the result of which is the processed data, given out in the PC port.

After the 25 cycle termination, the circuit is reset, and the reading address shifting by one digit is performed, that is , «sliding window» shift for the next pixel processing and the circuit operation is repeated.

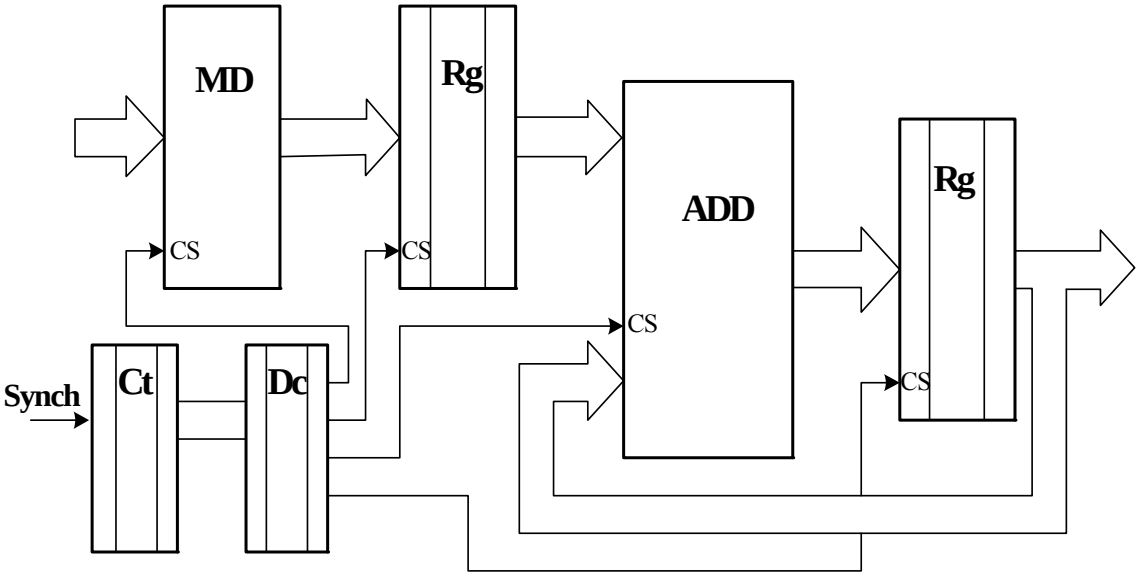

Figure. 2. Structural diagram of one-dimentional FPC-filter

In Figure 4 the time charts of one-dimensional filter operation modeling are shown, using the digital circuits simulation program - Modelsim SE PLUS 5.1.

The results of modeling confirmed that maximum operating frequency of three one-dimensional filters of edge detection, realized on the single-crystal PLIS Xc3s1000, is 41 MHz. The circuit uses all crystal resources, and for data array processing by "sliding window" of 5x5 size, less than 30 cycles are needed.

It means that for one pixel processing, the time of 0,73 μs is needed. Program realization of the same procedure using, for instance, the computer having the operating frequency of 3 GHz, the time of 3,9

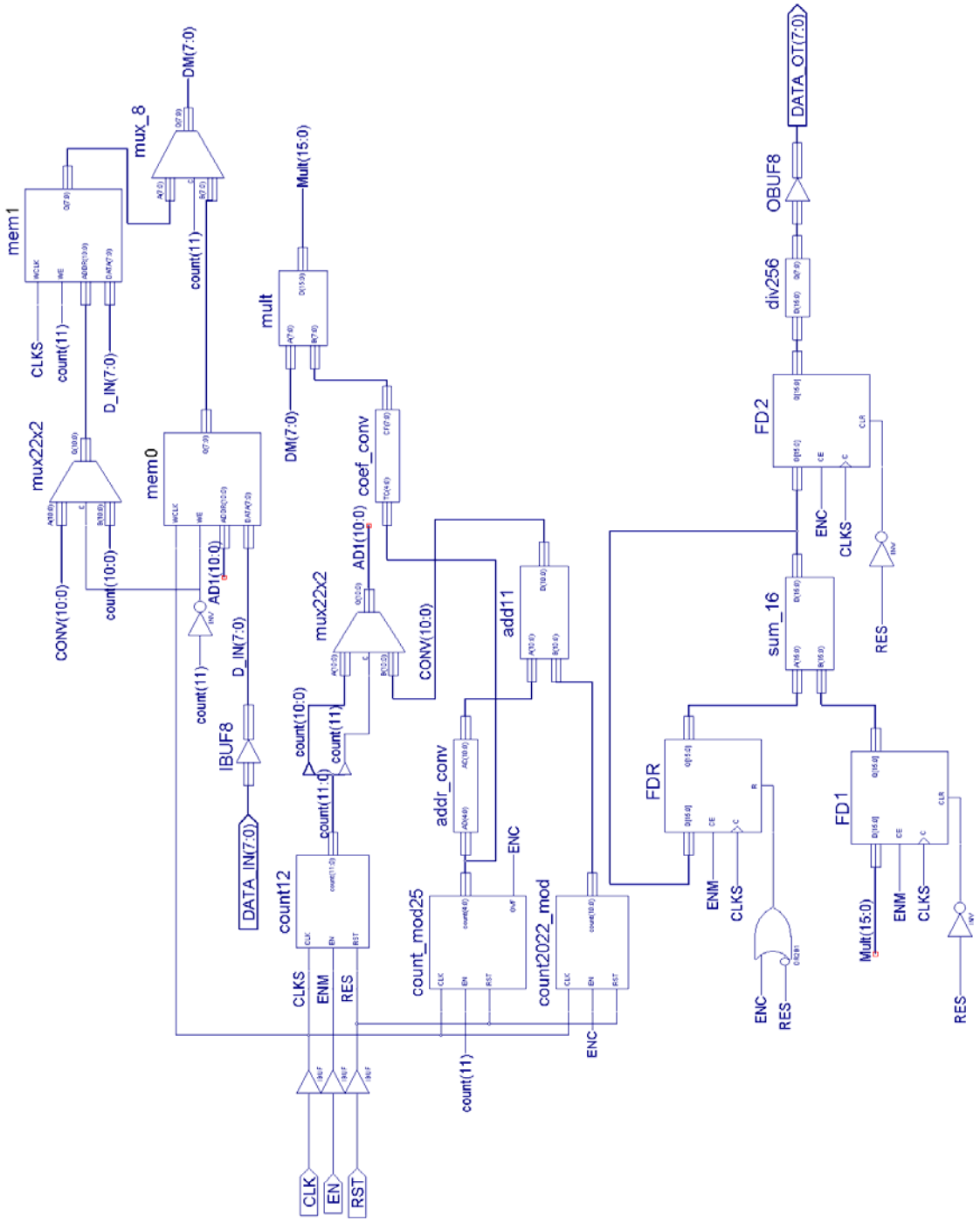

Figure. 3. Basic diagram of edge detector with one one-dimentional filter, using the Xilinx Project Navigator 7.1

μs is needed. It enables us to make a conclusion about the higher operating rate of the device, realized on PLIC, which grew 5,2 times.

Conclusions. The low-frequency Gauss filter of edge detector is realized on the base of PLIC Xc3s1000 family of Spartan-3. Such realization enables to improve operation rate, and can be widely used in the devices for preliminary images processing in large arrays of data.

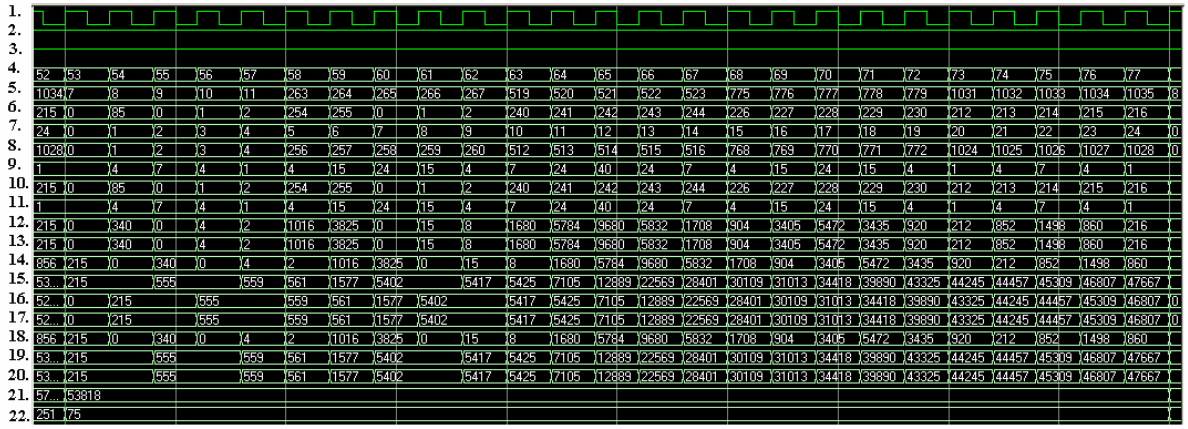

Figure. 4. One-dimentional filter modeling results, using the ModelSim SE PLUS 5.1program: 1) clock frequency CLK; 2) resolution signal EN; 3) reset signal RST; 4) data recording in storage mem1; 5) data read from storage mem0; 6) data read from storage mem0; 7) data of counter by 25 module count_mod25; 8) sliding window address addr_conv; 9) matrix coefficients transmitting coef_conv; 10) multiplexer data; 11) multiplexing coefficients; 12) multiplexing result mult; 13) multiplexing results recording in the FD1 register; 14) data reading from FD1 register; 15) recording data in the FDR register; 16) data reading from the FDR register; 17), 18) registers output data; 19) summation result sum_ 16; 20) summation result recording in the FD2 register; 21) data reading from the FD2 register; 22) division operation div256

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