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THE ANALYSIS OF TRANSMITTING FEATURE OF PUSH-PULL SYMMETRIC DIRECT CURRENT AMPLIFIER

The paper considers the principles of the push-pull symmetric current amplifiers building. The indicated method, despite the traditional asymmetric structure, stipulates fort the push-pull input cascade in the form of self-complete circuit with the common base, two symmetric intermediate cascades and push-pull symmetric output cascade. There had been deducted the equations for current transmission rate into separate amplifier's channels of push-pull symmetric constant current amplifiers, total current transmission rate for low signal zone and high signal zone, nonlinearity of transmission rate.

There had been given the simplified circuit of symmetric structure constant current amplifier. There had been proved that the circuits of push-pull symmetric constant current amplifiers have smaller error of linearity transmission rate.

Keywords: *CCA, symmetric structure.*

Introduction

The determinant features of analog circuitry are to be amplifiers, among which one can determine the separate group of direct current amplifiers (DCA), which in their turn are the basis for the operational amplifiers for analog and hybrid computing machines and measuring information systems [1]. The first DCA were designed using vacuum tubes [2]. At the same time the transmitting of approaches and structural schemes designing principles for vacuum tubes amplifiers to transistor ones has lead to the fact that DCA integral transistor schemes appeared within sixties and seventieth had been greatly similar to tube schemes. It was substantially limiting the approaching of maximum output within the frameworks of dynamic and static features as it was not allowing the usage of transistors frequency properties up to the boundary frequency f_T, also limiting the linearity of transmitting feature and number of the other parameters.

Urgency

A great number of dc amplifiers mainly use a single channel asymmetric structure consisting of differential amplifying cascade at the input and push-pull symmetric cascade at the output. At the same time there has been used the principle of currents amplification and transformation [3]. The advantage of such an approach is the functional universality of these schemes allowing their usage within different devices (operational amplifiers, buffer units, devices for analog signals selecting and storing, comparators etc.). Nevertheless amplifiers using differential cascade with a single channel structure have some disadvantages: the low speed of output signal intensification, substantial value of the non-linear distortions factor, particularly under the input signal frequency increasing, the skew ness of input signal working under the rectangular two pole input impulse.

It should be particularly mentioned the extremely high demands for the DCA used within multibit ADC and DAC included in high-precision information measuring systems, also hybrid computing systems, inasmuch as the final accuracy of transformations' results depends on the accuracy of input signal processing by the amplifier. Thus designing the schemes of DCA one should use the decisions satisfying the following demands: high linearity of statistic transmitting feature, current amplifying factor at the level of (10^4-10^6), low non-linear distortions factor (≤0,001%) under maximal bandwidth, minimal zero shift currents.

At the same time it should be mentioned that push-pull symmetric current amplifiers were started to design as early as in 70-tieth [4]. Nevertheless they were imperfect, because they had the limited number (1÷2) of amplifying cascades, low linearity and small transmitting factor. One of the

reasons for that was the complicatedness of necessary dc conditions setting within the above mentioned schemes with multi cascade structure (2÷3). Thus there was no any possibility to use the advantages providing by push-pull dc amplifiers of symmetric structure. Therefore the problem of push-pull symmetric dc amplifiers having the increased linearity of transmitting feature is to be **urgent**. The term «push-pull» means that the amplifying of two pole input signal (current, voltage) is made depending on its polarity by I or II amplifying channel in turn.

Aim

The aim of the paper is the analysis of transmitting feature factors of push-pull dc amplifiers of symmetric structure.

Tasks setting

According to the indicated aim the following basic tasks are formulated:

a) the interference of analytic correlations for the current transmitting factors within separate amplifying channels of push-pull symmetric DCA;

b) the analysis of general current transmitting factor for small-signal zone and zone of a large signal;

c) the non-linearity analysis of transmitting feature of DCA within the range of small and large signal.

Tasks solving

The dc amplifier enables to operate the direct current or voltage also slowly changing signals, particularly constant level signals. At present a number of the top world companies are involved in the designing of such DCA. The most well-known are: Analog Devices, National Semiconductor, Texas Instruments, Linear Technology, MAXIM, Philips, Pioneer, Inetrsil etc.

Nevertheless the amplifiers' structures produced by the above corporations are predominantly single channel, they have one transparent step-type amplifying channel and push-pull input cascade only. The authors suggest the designing of push-pull symmetric structure DCA.

Let's consider the simplest functional scheme of push-pull two cascades DCA of symmetric structure, represented on the Fig.1. It consists of input push-pull cascade, designed as the self additional scheme having the common base line with transistors T_1 and T_2. The bias voltages - U_{bias} and $+U_{bias}$ are transmitted to the bases of these transistors for working point rate setting. At the same time the summing point of transistors' T_1 and T_2 emitters is to be the system's input. The currents' sources I_3 and I_4 set the bias current within collectors and emitters of input transistors T_1 and T_2 correspondingly. DCA also contains push-pull two channel symmetric amplifying cascade, built upon the transistors T_3 and T_4. The summing point of these transistors' collectors is to be the amplifier's output. The scheme is connected to two power sources $+U_s$ and $-U_s$ accordingly.

Let's analyze the electric parameters of the given device. The total voltage drop within bias circles of the I-th cascade will be calculated using the formula $U_{\sum} = U_{bias} + \left| -U_{bias} \right| = U_{be1} + U_{be2}$ e.g. the sum of voltage drops at the crossovers base-emitter of the transistors T_1 and T_2, which in Eberth-Molle's approximation under $I_{in}=0$; $I_1=I_2 \approx I_0$ are calculated as:

$$U_{be1} = \varphi_T \ln \frac{I_1}{I_T}, \qquad U_{be2} = \varphi_T \ln \frac{I_2}{I_T},$$

where $\varphi_T = \frac{kT}{q} \approx 25\ мВ$ – thermal potential; $I_T \approx 10^{-15}$ A – heat current.

At the same time, as

$$U_{\sum} = U_{be1} + U_{be2}, \text{ then}$$

$$U_{\Sigma} = \varphi_T \ln\frac{I_1}{I_T} + \varphi_T \ln\frac{I_2}{I_T} = \varphi_T \ln\frac{I_1 I_2}{I_T^2}. \quad (1)$$

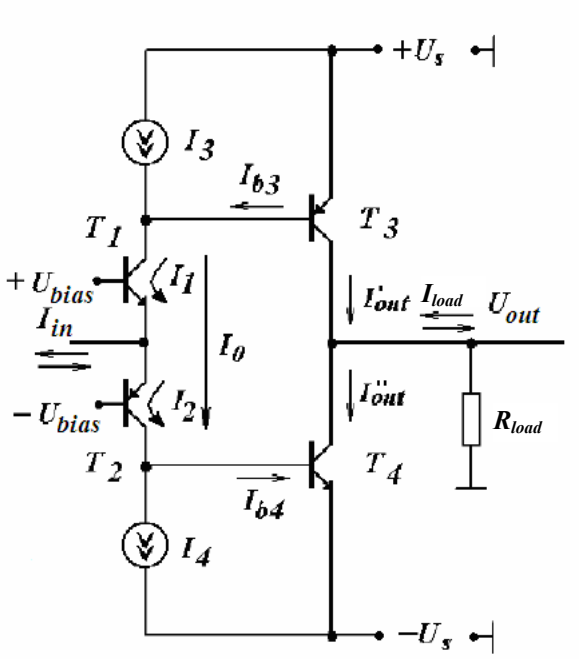

Fig. 1. The simplified functional scheme of push-pull two channel DCA of symmetric structure

Under the condition I_{in}=0, disregarding of I_{b1} and I_{b2}, we have $I_1 = I_2 = I_0$, where I_1, I_2– collector currents T_1 and T_2, and I_0 – transparent bias current within input cascade. Exponentiating (1) and considering I_{in}, we get

$$I_1(I_1 + I_{in}) = I_T^2 e^{\frac{U_{\Sigma}}{\varphi_T}}. \quad (2)$$

Under I_{in}=0 we have

$$I_T^2 e^{\frac{U_{\Sigma}}{\varphi_T}} = I_1^2.$$

Considering last equation and (2) we get:

$$I_1(I_1 + I_{in}) = I_0^2.$$

This formula is the basic equation describing the first cascade's currents increasing. Hence we find:

$$I_1 = -\frac{1}{2} I_{in} + \sqrt{\frac{I_{in}^2}{4} + I_0^2}. \quad (3)$$

Similarly:

$$I_2 = \frac{1}{2} I_{in} + \sqrt{\frac{I_{in}^2}{4} + I_0^2}. \quad (4)$$

The Fig. 2 shows the graph of I_1 and I_2 dependence from I_{in}. It illustrates how amplifier's input current is divided into components branching out to the collectors T_1 and T_2. The values I_1 and I_2 are determined by volt-ampere feature of transistors and depend on their power.

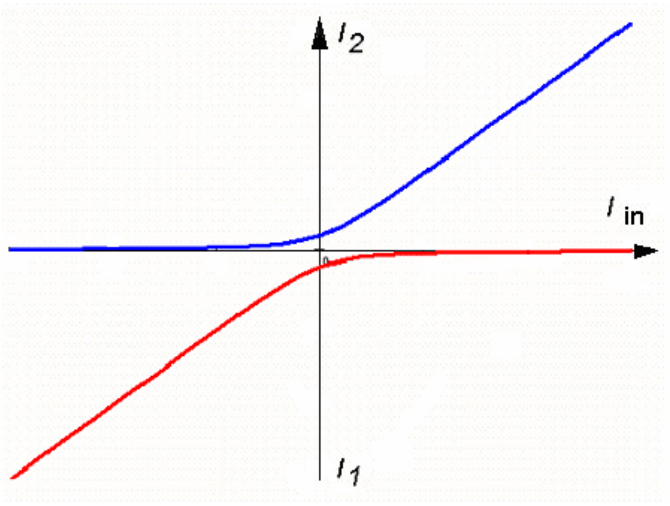

Fig. 2. Dependence of I_1 and I_2 from I_{in}

For currents increases $\Delta I_2=I_2-I_0$ and $\Delta I_1=I_1-I_0$ the dependence represented on the Fig.3 takes place

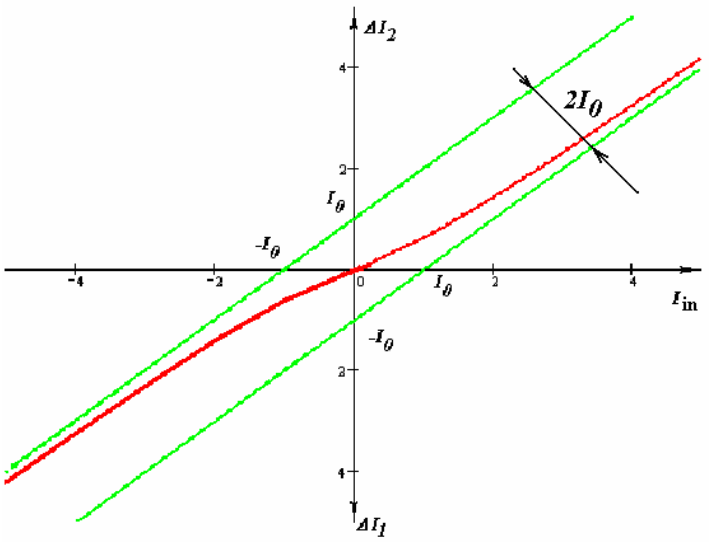

Fig. 3. The dependence of currents increases ΔI_2 and ΔI_1

It should be mentioned functions $\Delta I_1=f(I_{in})$ and $\Delta I_2=f(I_{in})$ have two zones:

1) $/I_{in}/\leq 2I_0$ – small-signal zone;

2) $/I_{in}/>> 2I_0$ – zone of large signal.

At the first zone: $\Delta I_2 \approx \frac{1}{2} I_{in}$. At the second $\Delta I_2 \approx I_{in} - I_0$

Let's consider the branching of $\boldsymbol{I}_{in}$ into components and its further passing through the channels of amplifying. At that:

$$I_{b3} \approx \alpha_1 I_1 - I_3,\ I_{b4} \approx \alpha_2 I_2 - I_4,\ I'_{out} \approx \beta_3 I_{b3},\ I''_{out} \approx \beta_4 I_{b4}.$$

Load current is formed as the difference of two components:

$$I_{load} = I''_{out} - I'_{out}.$$

Accordingly (4) and considering (2) we get:

$$I_{load} = \beta_4 \alpha_2 I_{in} + (\beta_4 \alpha_2 - \beta_3 \alpha_1) I_1. \qquad (6)$$

Using (6) and (3), we get:

$$I_{load} = \frac{\beta_4\alpha_2 + \beta_3\alpha_1}{2} I_{in} + (\beta_4\alpha_2 - \beta_3\alpha_1)\sqrt{\frac{I_{in}^2}{4} + I_0^2}\ . \qquad (7)$$

The expression (7) shows, that non-linearity of the first cascade is transferred to the output through the skew ness of amplifier's "arms". Under zero input current we have:

$$I_{load} = \beta_4\alpha_2 - \beta_3\alpha_1)I_0\ |_{I_{in}=0}\ .$$

That is why the initial current increase being equal to:

$\Delta I_{load} = I_{load}(I_{in}) - I'_{load}(I_{in})$, where $I'_{load}(I_{in})$ – value of I_{load} under I_{in}=0, is determined in the form of:

$$\Delta I_{load} = \frac{\beta_4\alpha_2 + \beta_3\alpha_1}{2} I + (\beta_4\alpha_2 - \beta_3\alpha_1)(\sqrt{\frac{I_{in}^2}{4} + I_0^2} - I_0)\ .$$

Function ΔI_{load} from I_{in} is represented on the Fig. 5.

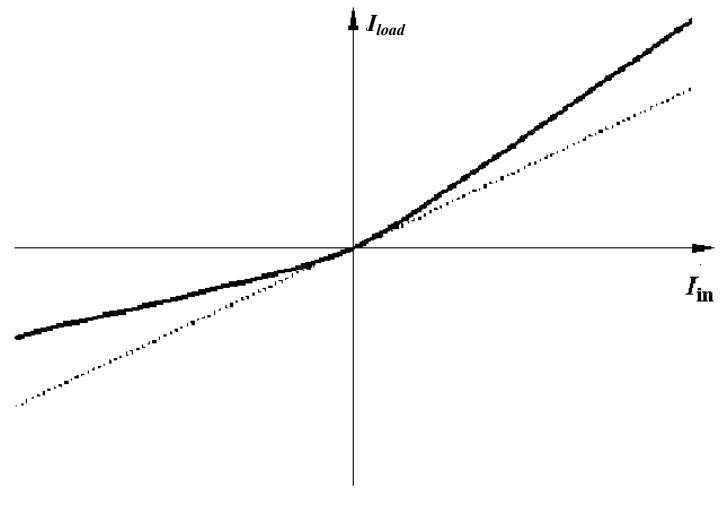

Fig. 4. The dependence of load current from I_{in}

The non-linear component of the dependence of an increase ΔI_n from I_{in} is marked as the dotted line:

$$\Delta I_{load} = \frac{\beta_4\alpha_2 + \beta_3\alpha_1}{2} I_{in}\ .$$

This equality takes place under the condition $/\mathrm{I_{in}}\ / \leq 2\mathrm{I_0}$ under $|I_{in}| << I_0$. At that $\Delta I_{load} \approx \beta_4\alpha_2 I_{in} - (\beta_4\alpha_2 - \beta_3\alpha_1)I_0$, and under $|I_{in}| << I_0$, $\Delta I_{load} \approx \beta_3\alpha_1 I_{in} - (\beta_4\alpha_2 - \beta_3\alpha_1)I_0$.

In case we take $\beta_4\alpha_2 > \beta_3\alpha_1$, at the graph it is shown as the increasing of the amplifying factor at zone of larger positive currents and its decreasing at zone of negative currents larger upon absolute value. All the above is accompanied by the displaying of small constant component of the initial current.

It should be mentioned that additional bias currents I_3 and I_4 at the circles of third and fourth transistor's bases can compensate only static part (4) of constant component of load current:

$$\beta_3 I_{b3} - \beta_4 I_{b4} = (\beta_4\alpha_2 - \beta_3\alpha_1)I_0\ .$$

But it is impossible to compensate the non-linear part of constant component in such a way, e.g. compensation at the expense of the second cascade bias is possible for separately small or large signal zone only.

The simplified practical principal DCA scheme of symmetric structure [6] is shown on the Fig. 5. Such an amplifier contains input push-pull cascade designed in the form of self adding scheme with common base on transistors T_4 and T_5. The working point of such a cascade is set by the voltage drop at the transistors T_1 and T_2 in diode engaging, which level is provided by currents' values of current generators I_1 and I_2. The scheme also contains two symmetric amplifying channels on the transistors T_{11} and T_{14}. Working points of these transistors are set by the paraphase current reflector leading into the scheme, and also current reflectors: upper – on transistors T_3 and T_7 and lower – on transistors T_6 and T_{10}.

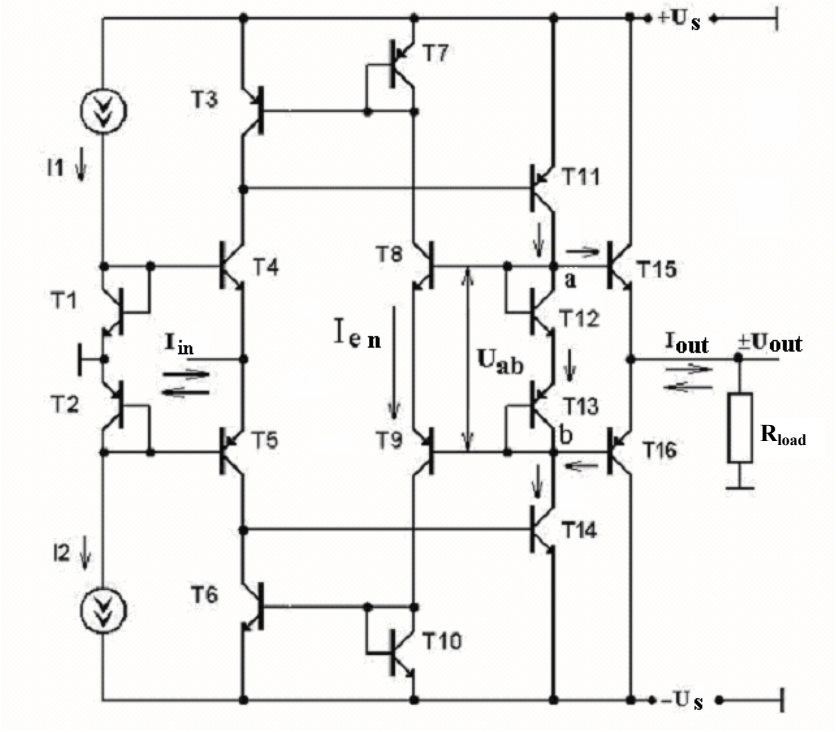

Fig. 5. Simplified principal DCA scheme of symmetric structure

The indicated principle of working point setting is provided by the transistors' T_{11}, T_{14} и T_7, T_{10} collectors' currents self balancing in diode engaging, also T_3 and T_4. In such a way, under the condition of I_{in}=0, $I_{K4} \approx I_{K5} \approx I_{K11} \approx I_{K14} \approx I_{K8} \approx I_{K9} \approx I_{K3} \approx I_{K6} \approx I_1 \approx I_2$. Following from the last correlation, it should be mentioned that transistors' working points of both upper and lower channels are set by the generators' I_1 и I_2 current levels.

The presence of paraphrase reflector at transistors T_8, T_9, T_{12}, T_{13} provides constant total potential difference U_{ab} at crossovers base-emitter T_{12} and T_{13} not only under the condition I_{in}=0, even when $I_{in} \neq 0$ and $I_{K11} \neq I_{K14}$. It should be mentioned that transparent $I_{e.н.}$ current through collector-emitter crossovers of transistors T_{15} and T_{16} is approximately equal to I_{K8} and I_{K9}. Growth ΔI_{out} ($I_{out} \neq 0$) is appeared under the condition when $I_{in} \neq 0$ and $I_{K11} \neq I_{K14}$ and $I_{K15} \neq I_{K16}$ and at the output differented current ΔI_n appears, creating non zero voltage drop U_{out}.

Amplifying factor of the given scheme for small-signal zone is calculated by the formula:

$$K_i = K_{i\,in} \cdot K_{PK} \cdot K_{i\,out} \ ,$$

where $K_{i\,in}$– amplifying factor of the input cascade current, calculated as:

$$K_{i\,in} = 0{,}5 \, .$$

K_{PK} – total average amplifying factor of intermediate cascade current at transistors T_{11} and T_{14}, calculated according to the formula:

$$K_{PK} = \beta_{p-n-p} + \beta_{n-p-n} \, ;$$

$K_{i\,out}$ – amplifying factor of the output cascade current, calculated in the form of:

$$K_{i\,out} = \frac{2 \cdot \beta_{p-n-p} \cdot \beta_{n-p-n}}{\beta_{p-n-p} + \beta_{n-p-n}}.$$

Then total amplifying factor within the small-signal zone is calculated by the final formula:

$$K_i = \frac{\beta_{p-n-p} + \beta_{n-p-n}}{2} \cdot \frac{2 \cdot \beta_{p-n-p} \cdot \beta_{n-p-n}}{\beta_{p-n-p} + \beta_{n-p-n}} = \beta_{p-n-p} \cdot \beta_{n-p-n}.$$

At that, for example, under $\beta_{\text{p-n-p}}$=50, and $\beta_{\text{n-p-n}}$=100 K_i =5000, coinciding the results of computer simulation. The increasing of the amplifying cascades number, correspondingly K_i increasing could be reached by the usage of paraphrase current reflectors separately at each cascade and one for few cascades. The application of symmetric design structure and paraphrase current reflectors in amplifying cascades gives the possibility to build high amplifying factors DCA: 100 db and more [6-8].

Conclusions

There had been derived the analytic expressions for the amplifying factors for input cascade, pre amplifying cascades and output cascade of push-pull DCA, allowing to evaluate the values of such factors using differential transmitting factors β for the current p-n-p and n-p-n of transistors.

There had been obtained the analytic correlations for the total current transmitting factor for small-signal zone and zone of large signal, giving the possibility of transmitting function analyzing of symmetric DCA input-output within the range of input and output signals.

There had been analyzed the non-linearity of the input-output feature. There had been shown this feature can be divided into the two components: the linear and non-linear ones. It allows to evaluate the non-linearity level of transmitting function depending on the values β diversity for p-n-p and n-p-n transistors.

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