UDC 681.3:621.375

A. D. Azarov, Dr. Sc. (Eng.), Prof.; A. A. Reshetnik, post-graduate

MATHEMATICAL MODEL OF COMPARATOR WITH REGULATED SENSITIVITY FOR FAST ACTING MULTIBIT WEIGHT REDUNDANCY ADC

Mathematical model of comparator with regulating sensitivity for fast multidigit ADC with weight redundancy is suggested

Keywords: *ADC, RPNS (redundant positional notation system), sensitivity regulation, comparator.*

Introduction

Traditionally successive approximation ADC is referred to medium speed devices. Therefore we can considerably improve high resolution SAR ADC speed using position notation systems with weight redundancy [1]. But for all that two aspects play important role: the weight redundancy level, which allows to compensate dynamic errors of I and II types [2] during successive approximation and due to this compensation to reduce cycle time; sensitivity and speed of comparator which is used. As a rule traditional ADC comparator sensitivity seems to be constant at all cycles and equals to half of the youngest quantum. Nevertheless this principle is unpractical for ADC with weight redundancy. In that case comparator sensitivity can be low at senior cycles whereas weight cycle duration is minimum. The comparator sensitivity must be high at younger cycles and cycle duration must be increased.

Actuality

Comparator sensitivity regulation enables considerably to increase the speed of SAR ADC with weight redundancy and high resolution [3] even relatively to method proposed in [1]. The comparator sensitivity is minimum difference of analog signal values which causes well-defined transition from one output logic state to another. So there are two sensitivity values: one for transition from 0 to 1 and the other- for transition from 1 to 0 . These values are equal but have different signs if zero shift would be neglected. Introduction of weight redundancy in ADC bit plane allows, due to regulation of comparison circuit sensitivity, to use variable cycle duration for speed enhancement. At the same time the above- mentioned approaches are non conventional, they are new and need addition investigations especially in the direction of defining dependence function of comparator sensitivity and comparator speed on input analog signals difference. Hence, the subject of the article dealing with the analysis of regulated sensitivity comparator mathematical model for fast acting SAR ADC with weight redundancy which fully binds comparator sensitivity with speed and approximation tact time cycle duration is the issue of the day.

Aim of research

The purpose of investigations is SAR ADC speed enhancing using comparator with regulated sensitivity.

Tasks

According to mentioned purpose current tasks are formulated:

Analysis of comparator static bitwise characteristic taking into account non sensitivity zone particularly hysteresis and noise.

Elaboration of the model of current comparison circuit taking into account transfer coefficient as a function of difference input signal.

Investigation of dependence of dynamic characteristics of comparison circuit with regulated sensitivity, particularly of transition process duration at different approximation cycles, depending on non sensitivity zone changes.

Problem solution

Weight redundancy appears in the case of certain relations between bit weights [1]. The sum of weights of younger bits must be greater than weight of senior i-th bit i. e. $Q_i < \sum_{0}^{i-1} Q_j$. The example of redundant notation system is the system with ratio $Q_i = Q_{i-1} + Q_{i-2}$ (Fibonacci digits) [4] or with bit ratio $Q_i / Q_{i-1} = \alpha$. In case of $\alpha \approx 1.618$ and $\alpha^i = \alpha^{i-1} + \alpha^{i-2}$ the system is "golden ratio system."

The structure scheme of SAR ADC with weight redundancy and variable cycle duration differs from ADC structure examined in [1]. The structure has comparator scheme with regulated sensitivity (CS) and regulated duration pulse generator (RDPG) for setting balancing cycles of different duration. The structure of such ADC for RPNS is shown in Fig. 1.

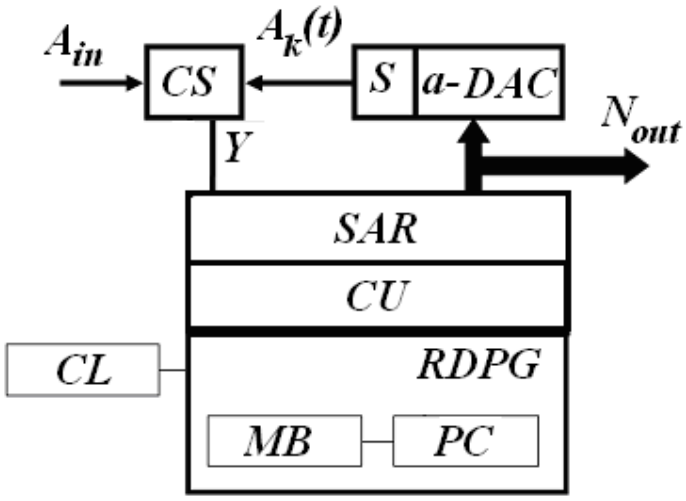


Fig. 1 Structure of fast acting SAR ADC with variable balancing cycle duration based on RPNS {0, 1}

The RDPG has CL – clock generator, MB – memory block and PC – pulse counter, α -DAC – DAC with weight redundancy, CU – control unit, LU – logic unit for output code $N_{вых}$ forming. The digital equivalent of output code N_{out} is defined as result of transformation A_{in} to $\sum_{0}^{n-1} a_i Q_i$? where a_i – the value of i-th bit $a_i \in \{1,0\}$.

It is necessary to note that building of multidigit (12-18 binary bits) fast acting SAR ADC is very difficult task. The main obstacle is that weight of youngest bit must be rather small. Moreover dynamic errors of I and II types and noises have considerable influence on device operation. For example, ADC with the number of bits n=18 and input signal range $D_{in} = \pm 2{,}5B$ has resolution 262144 quanta and at the same time youngest quantum value is 0.000019 V [5, 6]. At the same time

the sensitivity must be not worse than half of the youngest quantum. However serial comparators provide voltage sensitivity at the level of $U_{\min} = 5mV$ with time delay $t_{\max} = 4ns$ [7 – 10].

Due to application of variable duration of balancing cycles we can achieve considerable reduction of total balancing time . The balancing diagram for rapid A-D conversion with variable cycle duration for $\alpha = 1{,}618$ and $n = 7$ is shown in Fig. 2. In this case at senior balancing cycles the difference between input and compensation signals $\Delta A(t) = A_{in}(t) - A_{\kappa}(t)$ can be potentially great but at younger cycles the value of this difference decreases. Accordingly comparator sensitivity must increase gradually from senior cycles ((n-1), (n-2), . . .) to younger cycles (. . ., 1, 0) [11].

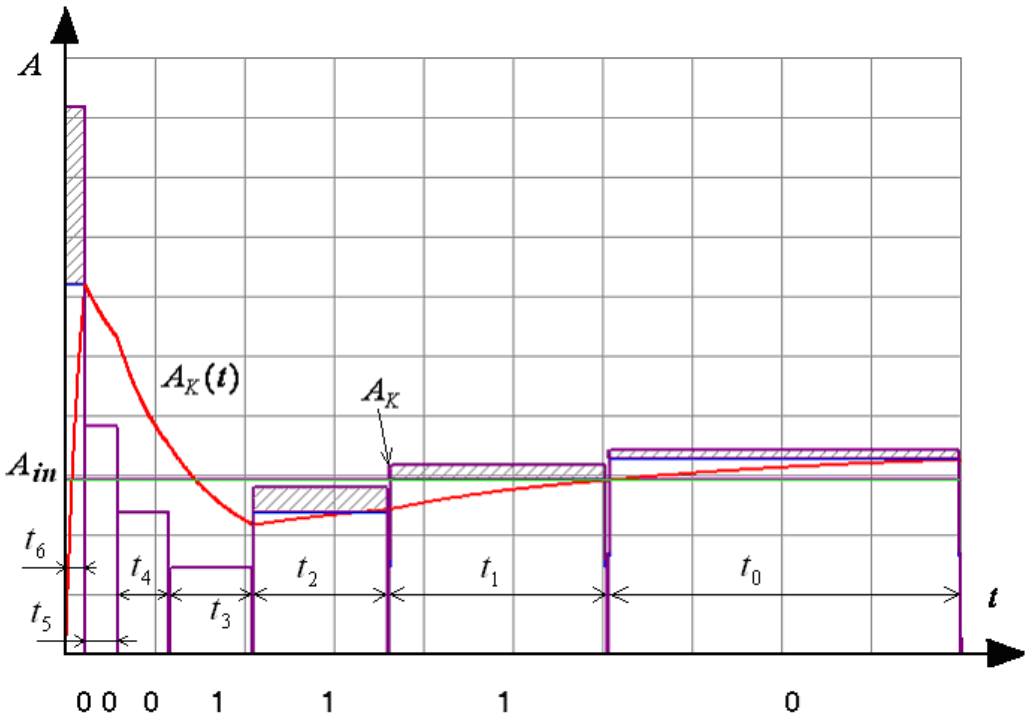


Fig. 2 Balancing diagram for forced conversion with variable cycle duration

At the same time cycle duration for senior (n-1)-th bit can be minimum and for the youngest bit (0) can be maximum. Balancing time is defined as:

$$T_{\text{var.}bal.} = \sum_{i=0}^{n-1} t_{T\,i} = \sum_{i=0}^{n-1} \alpha^{-i} t_{T\,0} = \frac{t_{T\,0}}{1-\alpha^{-1}},$$

where $t_{T\,0}$ - cycle duration of the youngest bit.

In case of constant cycle duration

$$T_{bal} = n_{\alpha} t_{T\,0},$$

where n_{α} – number of bits.

The advantage of application of variable balancing cycle duration as compared with successive balancing of constant cycle duration equals to

$$\gamma_{sp.\text{var}} = \frac{T_{bal}}{T_{\text{var}.bal}} = n_\alpha (1-\alpha^{-1}) = n_2 \frac{\ln 2}{\ln \alpha}(1-\alpha^{-1}) .$$

In case when transient processes in comparison circuit are determined by circuit function of the first order [1] then

$$\gamma_{sp} = \frac{T_{bal.2}}{T_{bal}} = \frac{(n_2+1)\ln\alpha}{-\ln(\delta Q + \alpha^{-n_a})},$$

where $T_{bal.2}$ – the balancing time for binary notation, δQ – the maximum value of assignment error.

The weight redundancy level δQ depends on RPNS type. As shown in [1] if $1.8 < \alpha < 2.0$ then the following formula can be applied for cycle duration evaluation .

$$\delta Q_i = \frac{\sum_0^{i-1} Q_j - Q_i}{\sum_0^{i} Q_j},$$

where Q_j - the weight of j-th bit. With increase of n_α $\delta Q \approx \frac{2-\alpha}{\alpha}$.

In that way the advantage of variable balancing cycle duration as compared with traditional binary balancing is defined by the expression

$$\gamma_{sp2} = \frac{T_{const.bal.2}}{T_{\text{var}.bal.}} = \frac{n_2(n_2+1)(1-\alpha^{-1})\ln 2}{-\ln(\delta Q + \alpha^{-n})} .$$

It is necessary to note that such equation allows only to evaluate the potential advantage regarding fast acting. . The real profit depends on many additional factors. The model of weight redundancy distribution between comparator and DAC is the most important factor. For values of notation system base α that is close to 2.0 the weight redundancy level is low and so the real profit in fast acting reduces . Nevertheless with increasing of weight redundancy level the profit is increasing too. The optimal distribution of weight redundancy depends several components particularly on the width of comparator static non sensitivity zone, transition function of comparison circuit and static error of analog units.

To obtain high sensitivity the comparison circuit must contain the threshold element (TE) in the form of standard voltage comparator, analog signals difference allocation device (DAD) and signal difference amplifier (DA) with nonlinear feedback. The structure must have adder for taking into account of noise influence. We will conventionally introduce signal adder to the structure for noise influence evaluation where noise ΔA_n is mixed(composition of thermal, shot, excessive, LF noise and other noises) to input signal. The whole structure is shown in Fig. 3. Analog signals difference $\Delta A = A_1 - A_2$ is formed at the output of DAD. Such approach allows us to assume that if TE has no noise then generalized noise equivalent appears at the DA output.

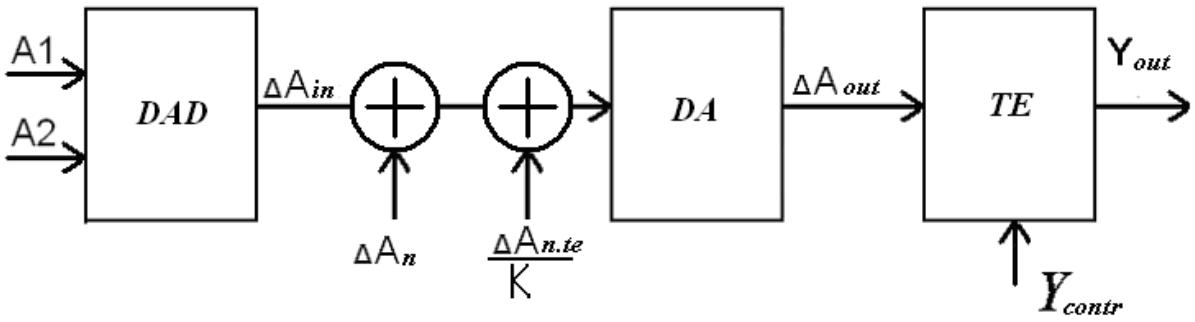


Fig. 3 High-sensitive analog signals comparison scheme

The CS operation time depends on the level of input difference signal. Operation time is constant for most of modern comparators (model AD8611 of ANALOG DEVICES company is typical example) [7]. In case of $U_{\max} \geq 5mV$ the comparator operation time is constant $t_{\min} = 4ns$, but with $U_{\max} = 1mV \div 5mV$ the operation time considerably increases. It is expedient to set such DA gain that $\Delta U_{out} \geq 5mV$ in order to provide reliable DA operation. In this case balancing cycle time will be determined mainly by dynamic characteristics of DA. As a rule the threshold characteristic of comparator contains hysteresis and is described as (Fig. 4) [12, 13]:

$$y_i = \begin{cases} 0, \; at \; \Delta A_{in} \leq -\Delta A_{Hi}/2 - \Delta A_{n\ TE} \\ 1, \; at \; \Delta A_{in} \geq \Delta A_{Hi}/2 + \Delta A_{n\ TE} \end{cases},$$

where ΔA_{Gi} – width of histeresis zone of CS at the i-th balancing cycle.

Quantitevly sensitivity can be evaluated via non sensitivity zone ($\Delta A'_H$) CCS. It depends on feedback resistance but at high resistance the influence of thermal noise increases

$$\Delta U_n = \sqrt{4kTR\Delta f},$$

where k - Boltzmann constant, T - temperature(K), Δf - frequency range.

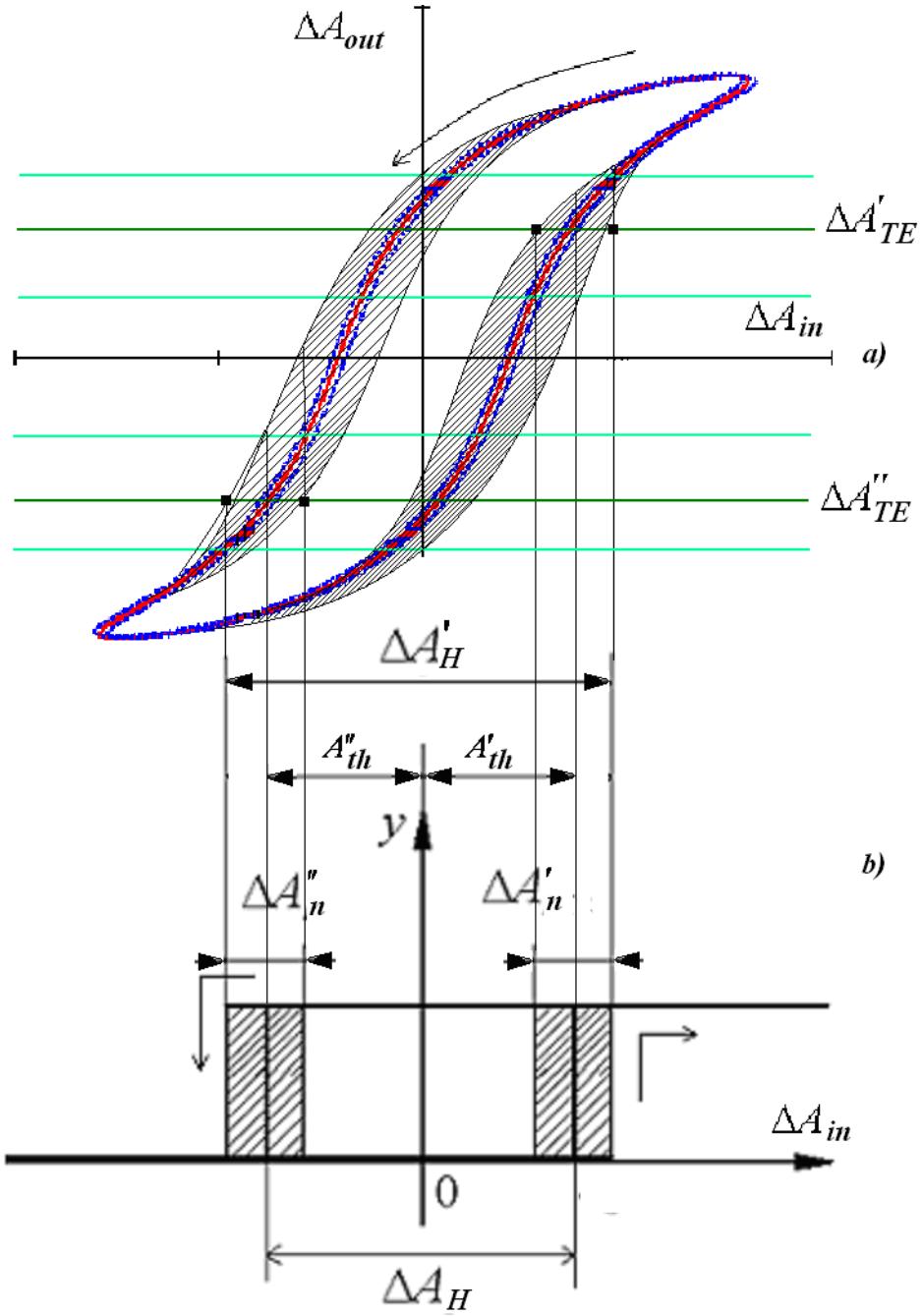


Fig. 4 Threshold characteristic: а) amplifier, б) current comparator scheme (CCS)

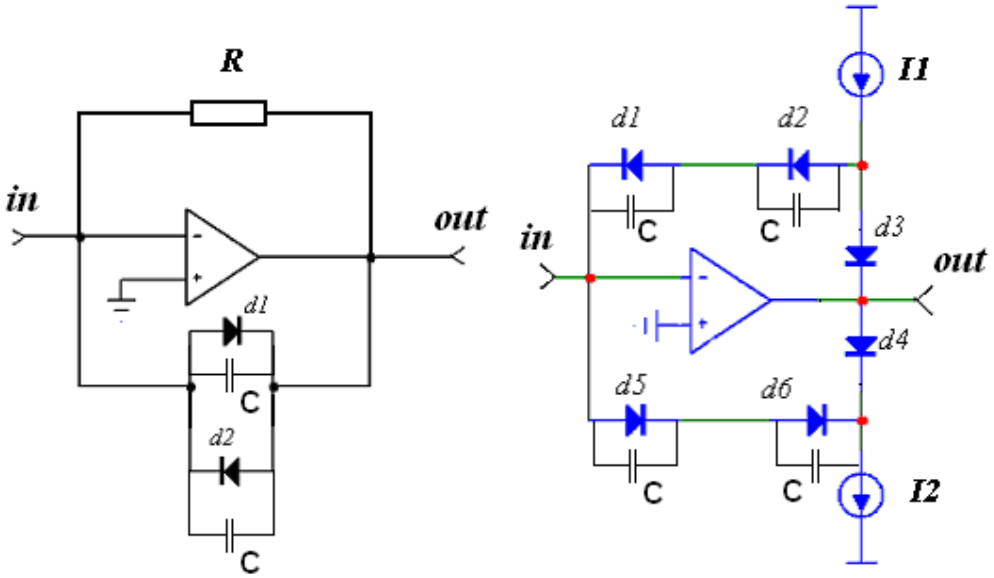
The geometric interpretation of hysteresis and DA noise superposition on comparator threshold characteristic is shown on the Fig. 4. The diagrams on the Fig. 4 are built regardless of zero shift effect (for simplification). The Fig. 4 a) presents hysteresis on the amplifier output. The hysteresis width ΔA_H determines the zone with not totally determined value on the comparator output. Availability of noise worsens the general sensitivity on $\Delta A_n = \frac{\Delta A'_n + \Delta A''_n}{2}$. The total hysteresis zone (dead space zone), taking into account noise availability $\Delta A'_H = \Delta A_H + \Delta A_n$, where $\Delta A_H = A'_{th} - A''_{th}$. In this case A'_{th} and A''_{th} are average of distribution of minimum excess of

zero level (sensitivity) during switching from 0 to 1 or from 1 to 0 accordingly which causes the transfer from one logic state to another. The amplifier decreases the general hysteresis of CS comparatively with TE hysteresis by K times (the gain factor has dimension of resistance because DA in this case is current-to-voltage converter). The amplifier noise is added to comparator noise which would decrease by K times. If amplifier has hysteresis we must add this hysteresis to the CS hysteresis. Hence the CS hysteresis zone width in general depends on hysteresises of amplifier and TE and noises:

$$\Delta A'_H = \Delta A_{H.DA} + \Delta A_n + \frac{\Delta A_{H.TE} + \Delta A_n}{K},$$

where ΔA_n - amplifier input noise, $\Delta A_{H.TE}$ - TE hysteresis.

The comparison of analog signals of regulation of amplifier transfer constant is realized automatically within the chosen schema. At the same time for changing of feedback resistance depending on ΔI_{in} it would be appropriate to use the peculiarities of diode volt-ampere characteristic [14]. The simplest variant of nonlinear feedback is the usage of two parallel diodes d1 and d2 (Fig. 5 a)) with subtractive polarity.



а) б)

Fig. 5 DA with regulated transfer constant and feedback in the form of: a) two forward connected diodes, b) diode bridge

In static mode the output voltage of the first circuit is determined by current through diode

$$U_{out} = -\varphi_T \ln(\frac{I_{in}}{I_0}),$$

where I_{in} - input current, $\varphi_T = 25mV$ - thermal voltage, $I_0 = 10^{-15} A$ - diode thermal current.

Other variant of non-linear feedback realization is diode bridge usage (Fig. 5 b)). Current values and number of diodes variation allow for different types of feedback and transfer characteristic. All input current flows thorough open feedback path. The output voltage shall be determined as

$$U_{out} = -\varphi_T \ln\left(\frac{I^2_{in}}{I_0(I_{th} - I_{in})}\right),$$

where $I_н$ - through current of current sources.

The amplifier reaction on rectangular signal can be defined as first type function [15]

$$U_{out}(t) = U_{out}(1 - e^{-\frac{1}{RC}t}).$$

Taking into account this equation the model of dynamic transfer characteristic of the amplifier with variable gain can be built.

Constant current amplifier with non-linear feedback in the form of diode bridge has some advantages while taking into consideration the presence of noise. Their feedback capacitance for such CCA is two times smaller. But this circuit has disadvantages. In case if I_{in} exceeds the level of sources I1 and I2 current the circuit will be out of operation mode. Circuit shown in Fig. 5 a) has large feedback capacitance at small values of input current. In addition the manufacturing of R resistance is very complicated and it is the additional source of noise, which has considerable influence on device operation.

The special current amplifier with internal non-linear feedback in the form of diode bridge can be used to overcome the above –mentioned drawbacks (Fig. 6). For circuits comparison the computer modeling was performed (Fig. 7). The transfer characteristics of the second circuit (Fig. 5 b)) and amplifier with internal non linear feedback (Fig. 6) are better than the first circuit characteristic (Fig. 5 a)). Such transfer characteristic is the best for development of comparator with regulated sensitivity.

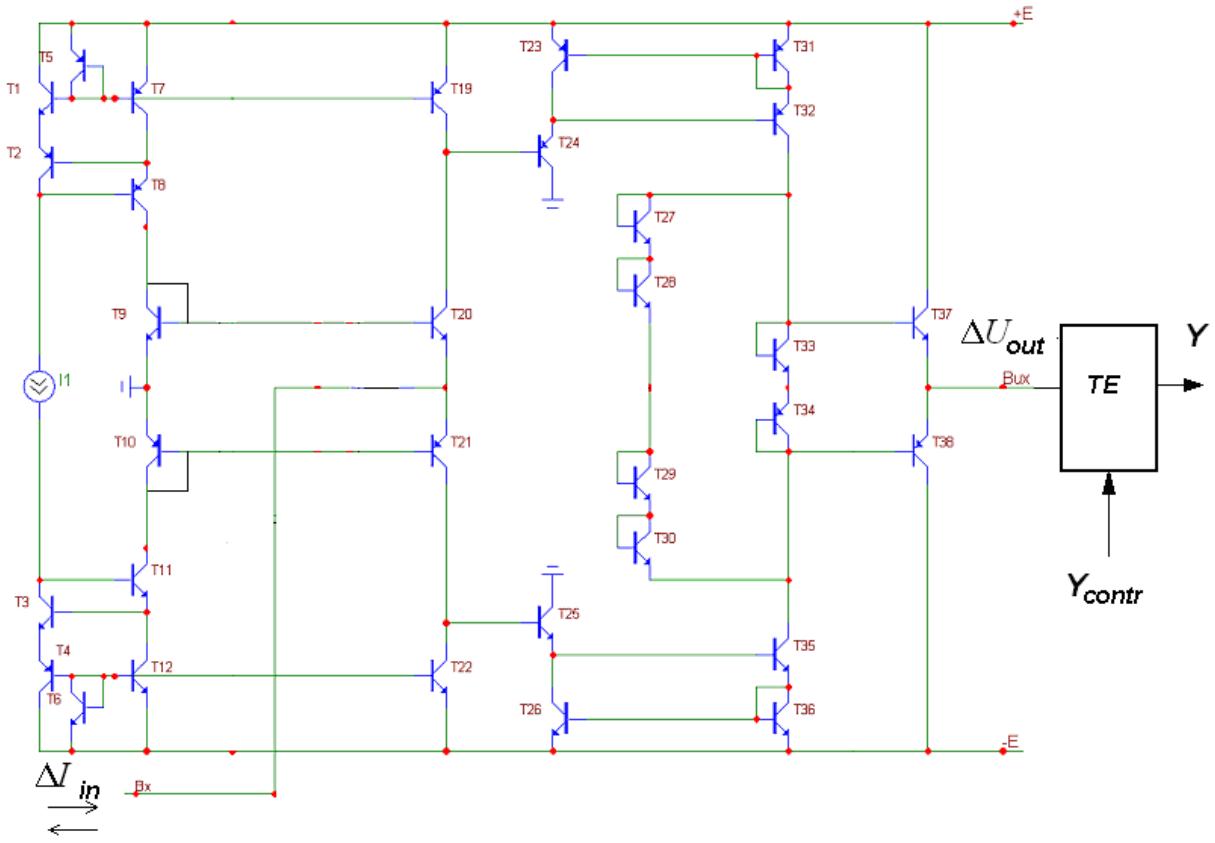


Fig. 6 Differential current amplifier with internal non-linear feedback

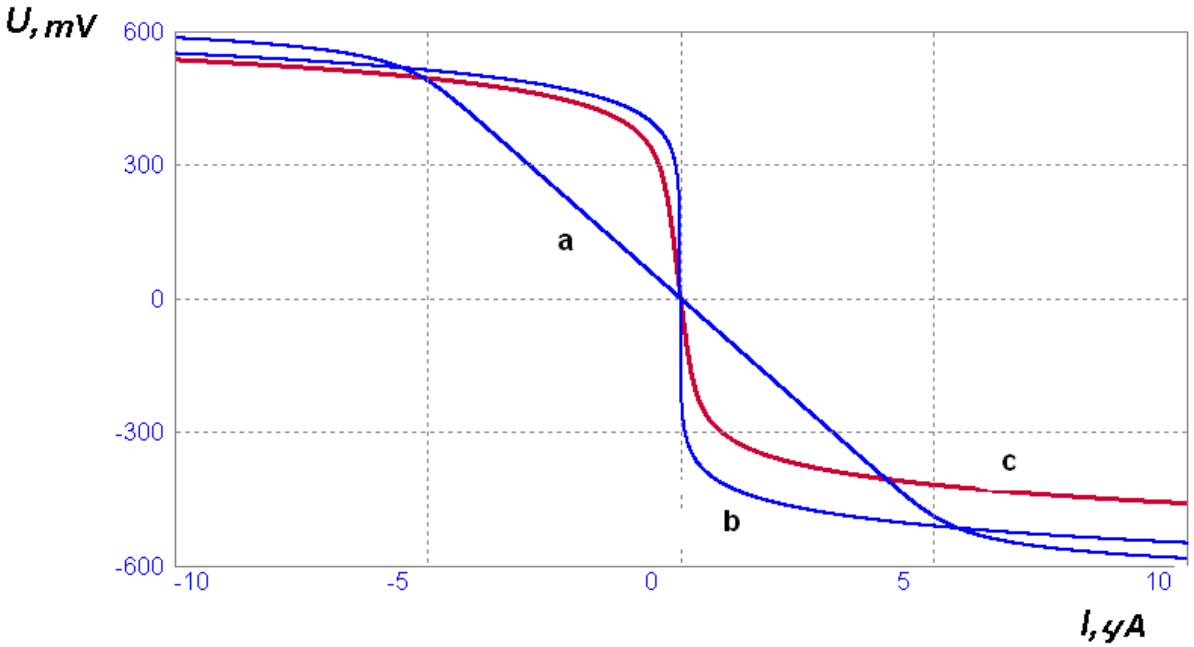
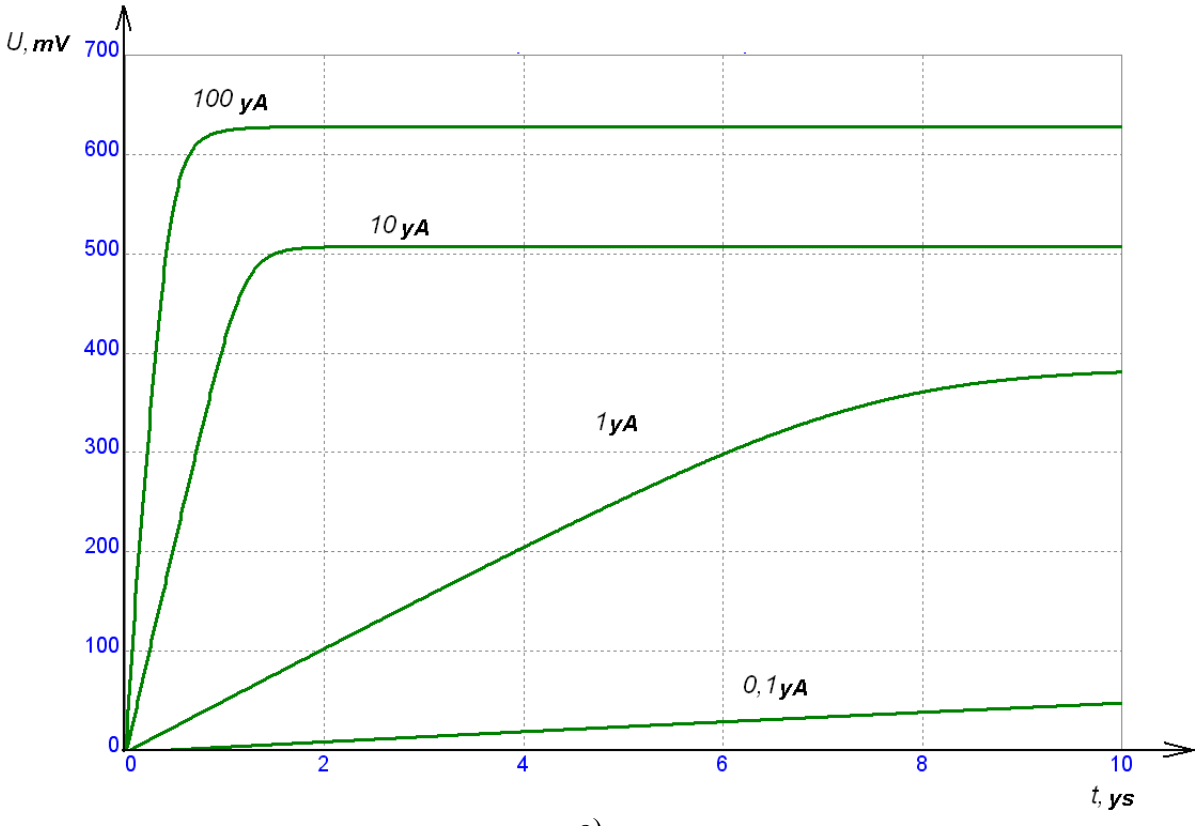
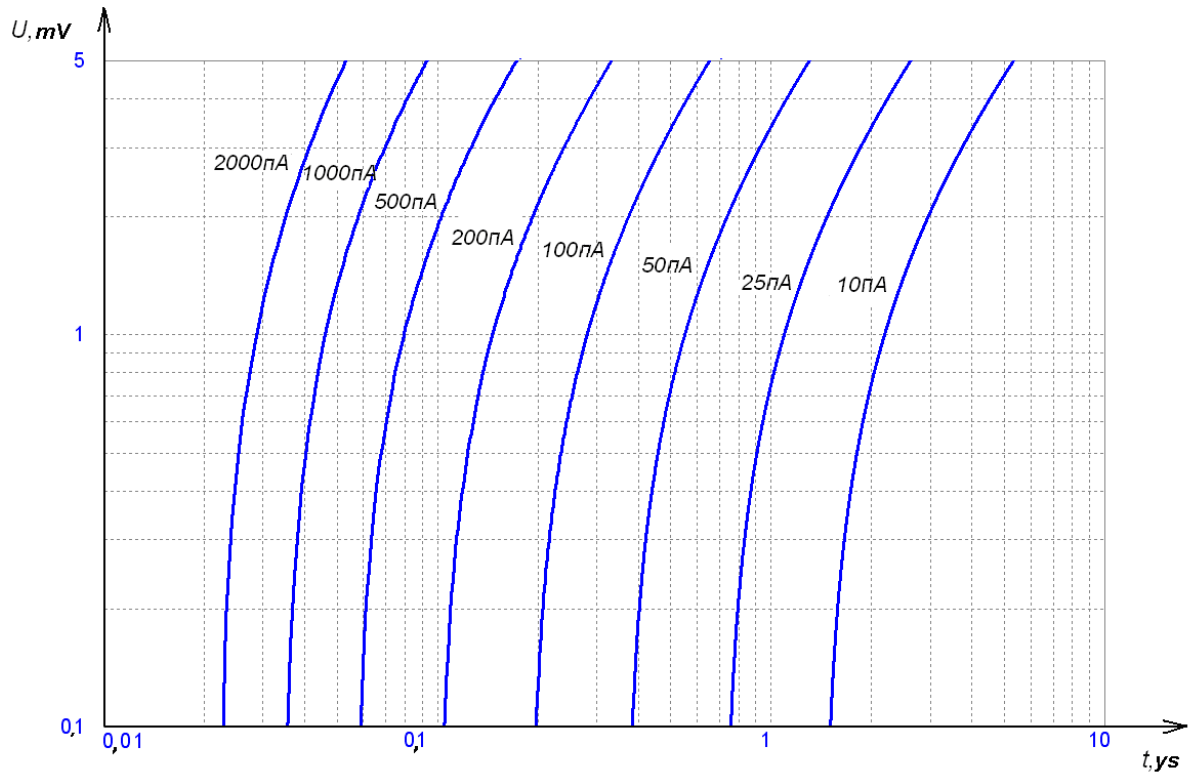


Fig. 7 Transfer characteristics of amplifier a) the first circuit b) the second circuit c) the circuit with internal non linear feedback



a)



b)

Fig. 8 Transfer characteristic of amplifier with regulated transfer constant with the different ΔI_{in} values: a) normal scale, b) logarithmic scale

For the amplifier on Fig. 6 there had been made the computer simulation of current comparator with modern integral models S700 [16]. There had been received the form of output signal of the amplifier with different input ΔI_{in} (Fig. 8). The graph is presented in the logarithmic scale on both axes.

Conclusions

1. There had been suggested the mathematical model of comparator with regulated sensitivity for fast multibit ADC with weight redundancy. The model realizes the dependence of comparator sensitivity on input signals difference values, dependence of operation time on sensitivity level as well as noise influence on comparator operation.

2. The suggested method of sensitivity regulation in ADC comparator allows to have the low sensitivity on elder conversion strokes, but the speed is high. At the same time the sensitivity is high on younger strokes and speed is low.

3. It had been proved that the usage of weight redundancy and current comparator sensitivity regulation allow to build the ADC with improved dynamic parameters. In this case the speed of the bit-by-bit transformation can be increased by 1-2 orders.

REFERENCES

1. Азаров О.Д. Основи теорії аналого-цифрового перетворення на основі надлишкових позиційних систем числення. Монографія. – Вінниця: УНІВЕРСУМ-Вінниця, 2004. – 260 с.

2. Островерхов В. В. Динамические погрешности аналого-цифровых преобразователей. – Л.: Энергия, 1975. – 176 с.: ил.

3. Захарченко С.М., Азаров О.Д., Харьков О.М. Самокалібровані АЦП із накопиченням заряду на основі

надлишкових позиційних систем числення. Монографія / Під. заг. ред. О.Д. Азарова. – Вінниця: УНІВЕРСУМ – Вінниця, 2005. – 235 с.

4. Стахов А. П. Фибоначчиевы двоичные позиционные системы счисления // Кодирование и передача дискретных сообщений в системах связи. – М.: Наука, 1976. – С. 155 - 179.

5. Analog-digital conversion / Edited by Walt Kester / Analog Devices Inc. 2004. 1230 pages.

6. B. Greben. Bipolar and MOS analog integrated circuit design. Published 2003 John Wily & sons Technology & Industrial Arts. 912 pages.

7. AD8611 8-Lead, Ultrafast 4 ns Single Supply Comparator. – Режим доступу: http://www.analog.com/en/prod/0%2C2877%2CAD8611%2C00.html – Заголовок з екрану.

8. HA-4900 Precision Quad Comparators. – Режим доступу: http://www.intersil.com/cda/deviceinfo/0,0,HA-4900,0.html – Заголовок з екрану.

9. TLV-3501 4.5ns Rail-to-Rail, High Speed Comparator in Microsized Packages. – Режим доступу: http://focus.ti.com/docs/prod/folders/print/tlv3501.html – Заголовок з екрану.

10. LMH7220 - High Speed Comparator with LVDS Output from the PowerWise® Family. – Режим доступу: http://www.national.com/pf/LM/LMH7220.html – Заголовок з екрану.

11. Азаров О. Д., Решетнік О.О., Захарченко С.М. Підсилювач з регульованою чутливістю для схеми порівняння струмів // Інформаційні технології та комп`ютерна інженерія.– 2005.– N2.– С. 5 - 13с.

12. Красносельский М.А., Покровский А.В. Системы с гистерезисом. – М.: Наука. Главная редакция физико-математической литературы, 1983. – 272 с.

13. Alexei Pokrovskii. Systems with histeresis. – Режим доступу: http://euclid.ucc.ie/hysteresis/node2.htm – Заголовок з екрану.

14. Степаненко И.П. Основы микроэлектроники: Учебное пособие для вузов. – М.: Сов. радио, 1980. – 424 с.

15. Сигорский В.П., Петренко А.И. Основы теории электронных схем. – К.: Техника, 1967. – С. 469 – 481.

16. 700 Series 20V Bipolar array design manual. – Режим доступу: http://www.arraydesign.com/_count/countdown.cgi?7MANUAL.PDF – Заголовок з екрану.

Azarov Alexey Dmitrievich – Director of Information technology and computer engineering Institution, Head of computer engineering department;

Reshetnik Alexandr Alexandrovich – post graduate student of the Department of computer engineering.

Vinnitsa national technical university;