

I. V. Slobodian

CGS-BASED NONVOLATILE MEMORY PROGRAMMING SPEED

The paper studies the influence of a set of factors on the speed of programming the nonvolatile memory (NVM) based on chalcogenide glassy semiconductor (CGS). The method is described for determining the speed of programming the device switching on (crystallization, low-resistance state) and switching it off (amorphization, high-resistance state). It is also shown that the speed of switching off and on the NVM depends mainly on the electric contact of the device.

Keywords: phase change, on /off switching speed, crystallization-amorphization.

Introduction

CGS-based nonvolatile memory (NVM) changes its phase state from high-resistance to low resistance state and vice versa under the influence of electric signals. It is believed that such NVM could, potentially, replace the existing types of nonvolatile memory, even those, which have high information exchange speed and operation stability, and to exceed their performance. Chalcogenide glassy semiconductor (CGS) used in this NVM has no fundamental limitations of the overwrite speed – up to sub-nanoseconds and in terms of the size of memory cells (MC) – up to 50 angstroms. Among the advantages we can mention the fact that the achieved overwrite current level does not damage the memory and reduce overwrite cycles as it was the case with the first samples of the memory.

The technology of phase changes in CGS (GeSbTe), that was invented and developed by Stanford Ovshinsky, was quickly commercialized in the field of nonvolatile memory [1]. This process was accelerated due to the efforts of many research teams [2]. Conductivity rather than reflexivity is the main characteristic of the given semiconductor alloy, which, ultimately was the main reason for selecting CGS as the basic material for new-generation NVM. There is a broader range of various composite alloys of CGS, used for NVM, than the spectra of those used for PC optic devices [3].

NVM technology for PC is based on phase transformations in semiconductor environment with volumetric negative differential conductivity of S-type (S-NDC) that exists due the high density of current filaments, which causes the semiconductor phase change [4]. There is a generally accepted view that current filament in NVM device is well-formed and its dynamic resistance is zero. Hence, any deviation from zero indicated by a measuring device (dU/dI for the overwrite current range) is determined by the total sum of all resistors connected in series between the probes including resistance of the contacts.

In optical memory the programming power (of recording, erasing, overwriting) is applied directly to the surface of the information storage device using a laser beam. In the electric storage devices energy is transmitted via the electric signal passing through the metallic or semi-metallic contacts [2, 4]. S-NDC increases the role of inhomogeneities and has the ability to maintain a stable state of low and high resistance without the application of external energy [4]

Knowing the material of contacts and geometry of the device, we can obtain volt-amp characteristic of on / off switching of NVM that, as a rule, coincides with practically obtained values of resistance of the contacts and does not depend on the thickness and temperature of chalcogenides.

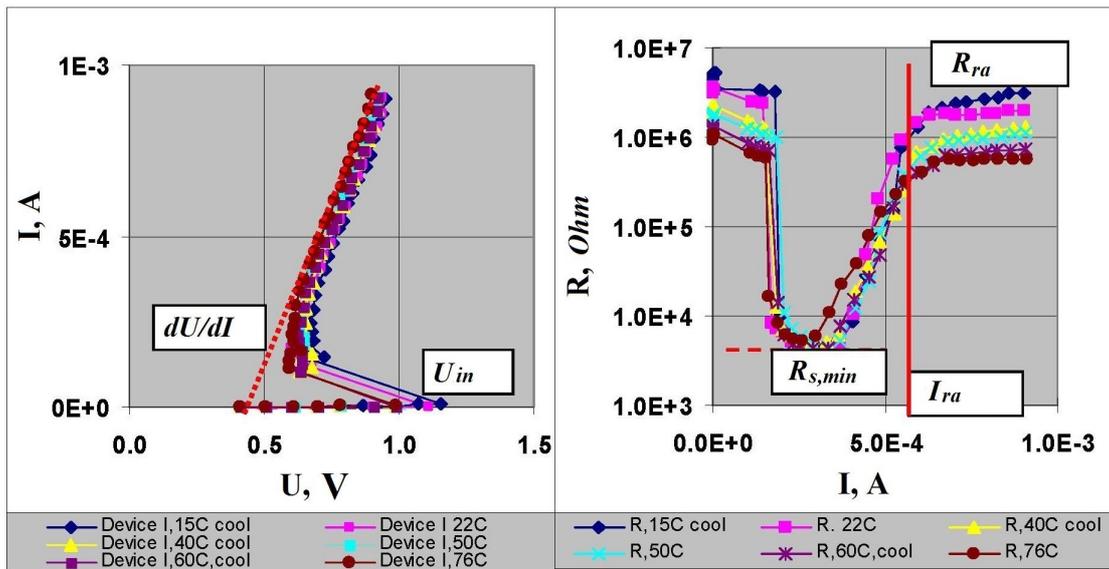


Fig. 1. Volt-amp characteristic of a standard CGS-based NVM of BDL type for the sample of alloy № 225 (Ge₂Sb₂Te₅) with carbon contacts

Fig. 1 shows typical R/I and I/U dependences for NVM at different temperature values. Such instruments are of a “breakdown” type, which is described in [2]. All of the data, given below, are taken from the published practical modeling results with informational purposes and for obtaining specific expressions. Saturated current values (I_{ra} , red line) for off-resistance (R_r) and resistance values in the minimum curve of R/I dependence (dotted line) indicate the on-resistance (R_r), obtained by electric low-field measurement of the sum of all the resistances between the probes – R_s and resistances of the contacts – dU/dI . Thus, minimum value of the chalcogenide material in MC will be given by

$$R_{HGS,min} = R_{s,min} - dU/dI, \tag{1}$$

where dU/dI is measured by the slope of I/U dependence curve with off-current from 50% to 100% (erasing) due to the possible non-linearity of the process.

This paper *aims* at studying the influence of overwrite current level, phase change in the composite alloy sample and its thickness, contact materials of the electrodes, geometry of the device and the temperature on NVM programming speed.

Experimental part

NVM operates on the basis of the “breakdown theory” with formation of the structure of current channels, which leads to conductivity changes. All information about modern devices with chalcogenides, used as a memory layer manufactured using electron-beam lithography (EBL) with formation of an electric breakdown layer (BDL), is of experimental origin [3].

Off-speed measuring method. Memory erasing speed is usually measured using optimized electric on-pulses and changing the duration of optimized off-pulses as shown in Fig. 2.

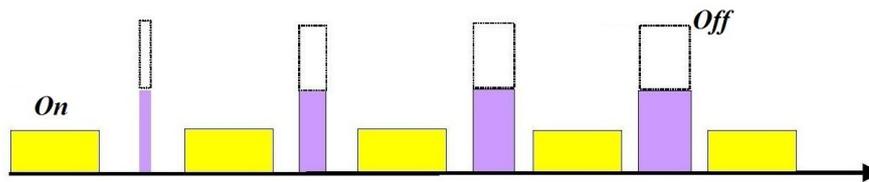


Fig. 2. Scheme of the erasing speed test; fixed on-pulses (duration and amplitude) and off-pulses (amplitude)

The optimized amplitudes are calculated on the basis of data obtained from measuring volt-amp characteristic of the real device. Information is collected from its amplitude values, used as the parameters, by changing the erasing pulse duration from 10 ns to 500 ns.

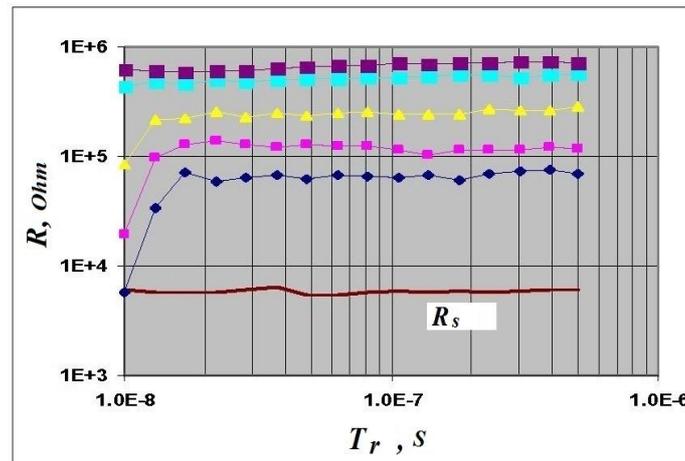


Fig. 3. Example of $R_r.t/Tr$ plot with different off-amplitudes

Resistance of low-field devices is measured at direct current supplied with a slight change after each pulse. Finally, erase speed is determined as I_r / I_{r_a} ratio when T_r drops below 20 ns. In this case saturation current reaches its nominal value and initial off-resistance is selected from the interval of 1 kOhm - 1000 kOhm.

On-speed measuring method. Fig. 4 shows the results of testing a memory cell. From the moment of switching on the device, the required on-resistance value (R_{s_0}) is reached almost immediately. The next off-amplitude value increases (off-pulse duration remains fixed throughout the test). Then, in order to switch the device on, increasingly broader on-pulses are supplied to it, which leads to ever faster phase changes of the device.

The required on-resistance value is determined as follows:

$$R_{s_0} = 10^{\{\log(R_s) + [\log(R_r/R_s)]/6\}} \quad (2)$$

Calculation results are presented in Fig. 5.

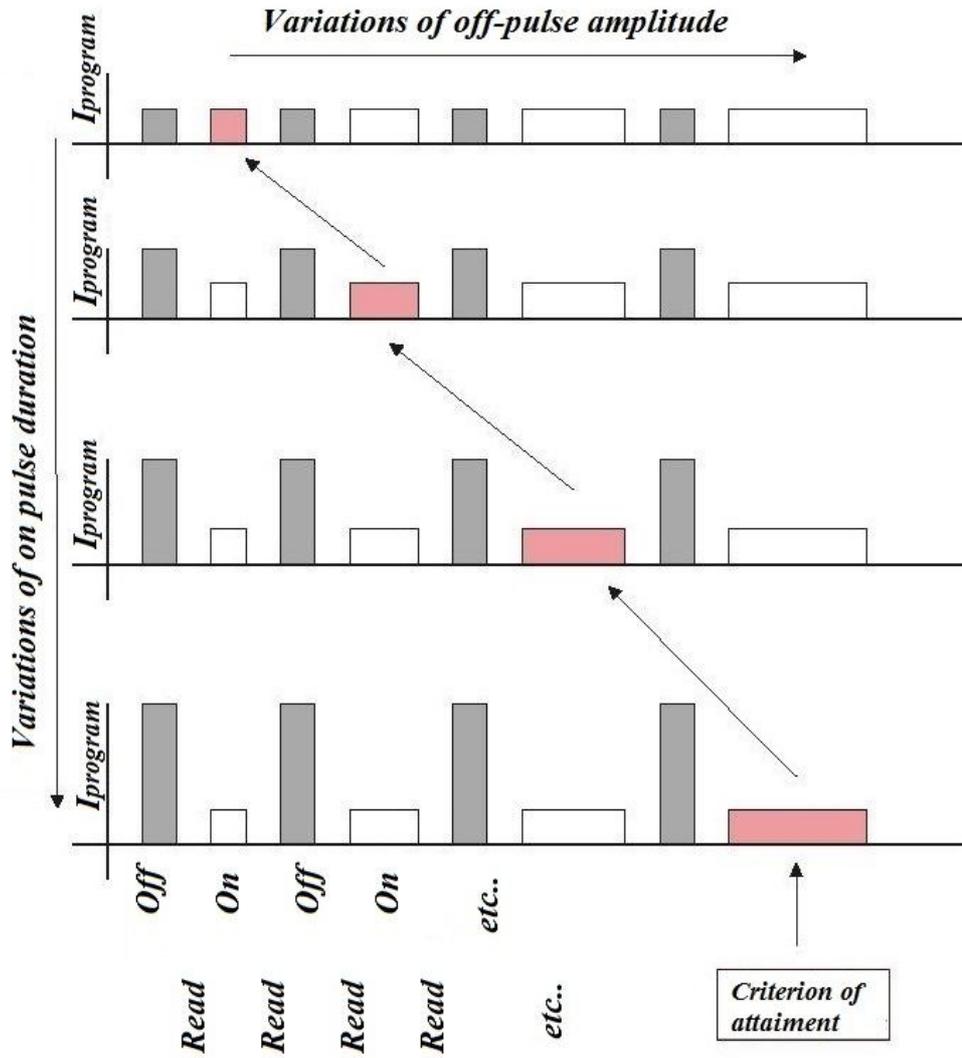


Fig. 4. The scheme of on-speed determination test

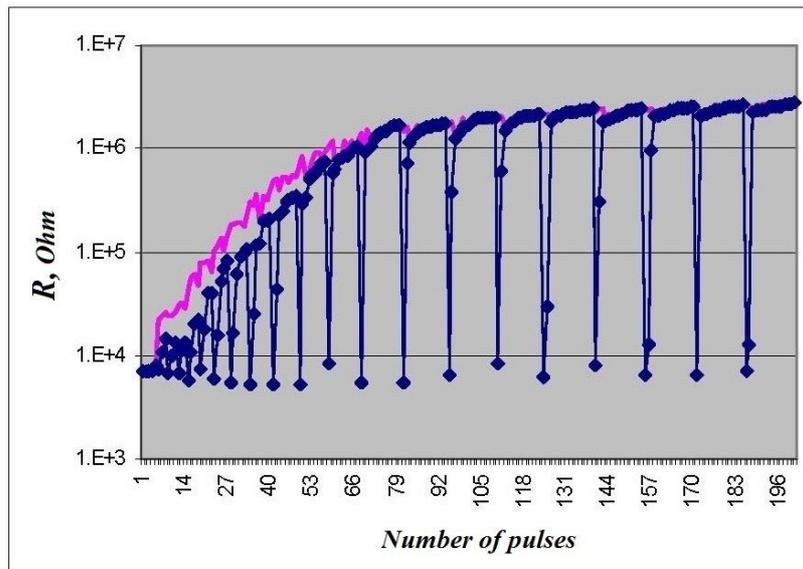


Fig. 5. Example of output data

Results and discussion

The above-presented results deal with experimental studies of the kinetics of CGS phase changes from amorphous to crystalline state for the film sample of GST № 225 with the thickness from 13 to 100 nm. First, it should be shown that off-resistance of the device of the current channel type can be calculated from a geometrical figure in the form of an inverted cone with a cut vertex. In such case resistance will be calculated by the formula [2]:

$$R = (\rho \cdot d) / (\pi \cdot r(r + d/\operatorname{tg}\alpha)), \quad (3)$$

where r is the radius of the lower contact, d – thickness of CGS film, α is associated with current filament and is assumed to be 45° .

Fig. 6 presents experimental data and scaling of Rr_a relative to the thickness of CGS film.

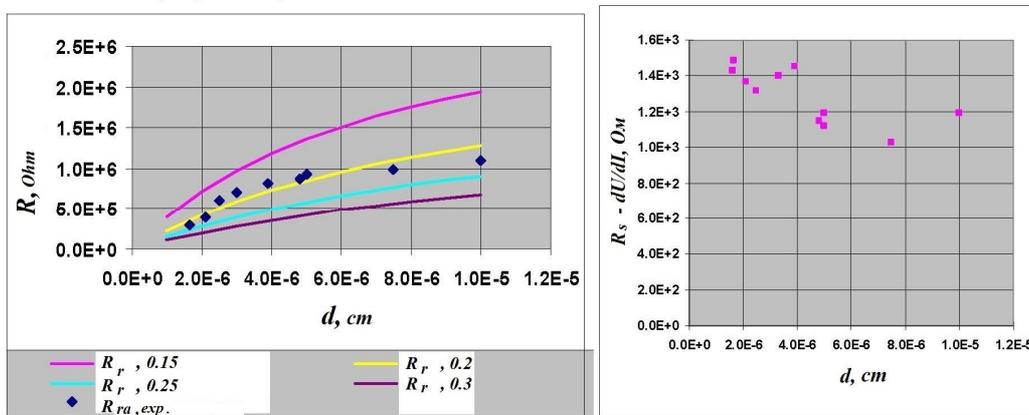


Fig. 6. Calculated and experimental values of Rr_a and scaling graph $R_s - dU/dI$ relative to d

It is evident that Rr_a satisfies the above expression when the diameter of the current channel $2r = 2000$ angstrom. Comparison of the threshold voltage of switching NVM MC with the thickness of CGS film [3] has also confirmed that the entire thickness of the device is concentrated in the phase transition region. On the other hand, on-resistance R_s after subtracting dU/dI is not comparable with thickness d of HcGS film. This is the evidence of the presence of a layer with high value of a low-resistance specific voltage that does not depend on CGS thickness.

And now let us consider “crystallization time” that is determined by duration of on-pulses necessary for the device to reach the required resistance level at which switching off begins as it is shown in Fig. 7 [2]. Off-pulse duration is 20 ns. At the moment when the device almost reached on-stage, the necessary duration of on-pulses grows practically in geometrical progression:

$$T_s = T_{s_{\min}} \exp(G \cdot R_r), \quad (4)$$

where G is conduction characteristic with a certain intermediate saturation changing in a vertical direction similar to Rr .

Growth of the on-pulse duration is observed when the residual number of fractions of crystal particles in the device is reduced. It is believed that vertical growth of pulse duration occurs at the off-resistance in accordance with the loss of crystal structure clusters. It is worth mentioning that T_s is not only crystallization time but also the time of reaching a definite value by the entire crystalline region and creation of the closer contact with the electrode interface in order to reach the necessary resistance R_{s_a} for full switching of the state.

$T_{s_{\min}}$ is known to change proportionally to the thickness of CGS film [3], which allows us to assume that crystallization front spreads through the volume of CGS between the contacts along the

current path at an approximate speed of 600 cm / s. Thus, on the one hand the minimum resistance R_{CGSmin} of the film of chalcogenide semiconductor is not proportional to the thickness but, on the other hand, crystallization of the material spreads from one contact to another. These two observations, taken together, make it possible to suggest that crystallization region, localized on one of the contacts, is primarily responsible for R_s .

The value of the amplitude of on-pulse with increased duration of U_{s0} , the graph of which is shown in Fig.7b, should be set below the product of the required resistance value R_{s0} and off-current I_r . RI curve is presented in Fig. 7.

$$U_{s0} < R_{s0} \cdot I_r \quad (5)$$

The value of the saturation resistance R_r is determined directly from the volt-amp characteristic of the device and the values of saturation off- and on-currents, I_{ra} and I_{sa} , should be 20% above the critical values at which the material of NVM layer passes from one phase to another.

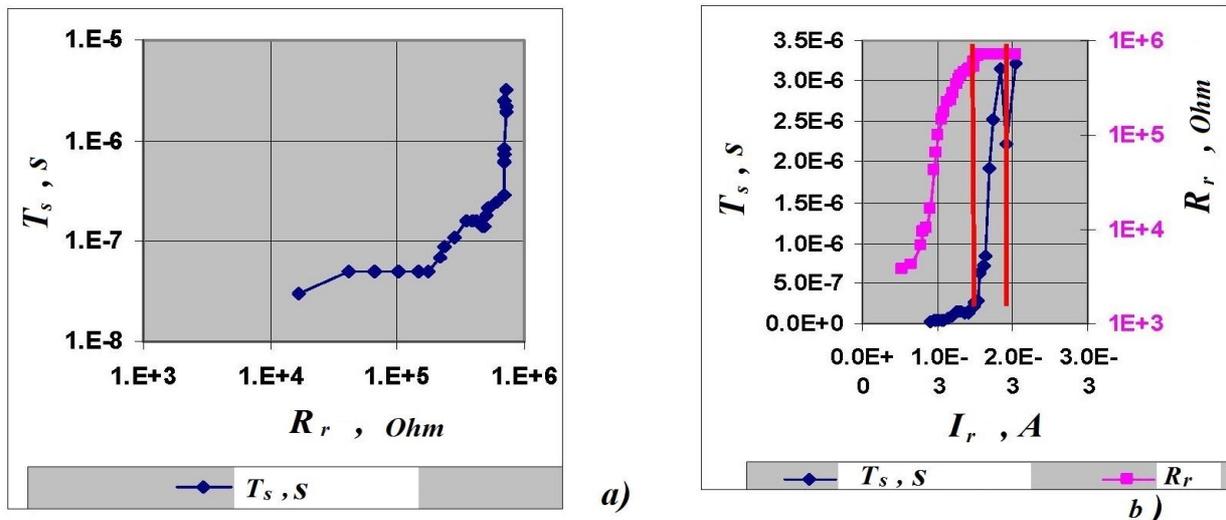


Fig. 7. Dependence of the on-pulse duration on the off-resistance (a) and programming current (b). The device has BDL-structure with reactive contacts of C – C type

Let us assume that dominating part of R_s is located on the surface of the electrode and crystalline material serves as an artificially formed (virtual) contact with CGS film. Then, the effective area of the virtual contact with the electrode will depend on the low-field resistance of the electrode and $R_{off.nes}$. The highest resistance is observed when in CGS volume there is maximal amount of the crystalline material. Minimal value of $R_{off.nes}$ also requires maximal fraction of the crystalline material. If resistive electrode is used, the percentage of the crystalline material in CGS film will be lower. Thus, the presence of a resistive interface, formed from a carbon of C-C (carbon – carbon) type reduces the effect of shunting crystalline “current filaments” in the amorphous material.

Let us consider the problem of how the on-speed of NVM device could be changed. It is natural to suggest that ohmic contact installation (low resistance) would lead to the reduction of R_s , U_{in} и T_s . There are several alternatives: to change the alloy composition with the same materials of the contacts, to change material of the contacts, to introduce an intermediate contact layer with low ohmic resistance between CGS and the main electric contact or to combine these methods.

Table 1 presents some experimental data [2].

Table 1

Experimental data

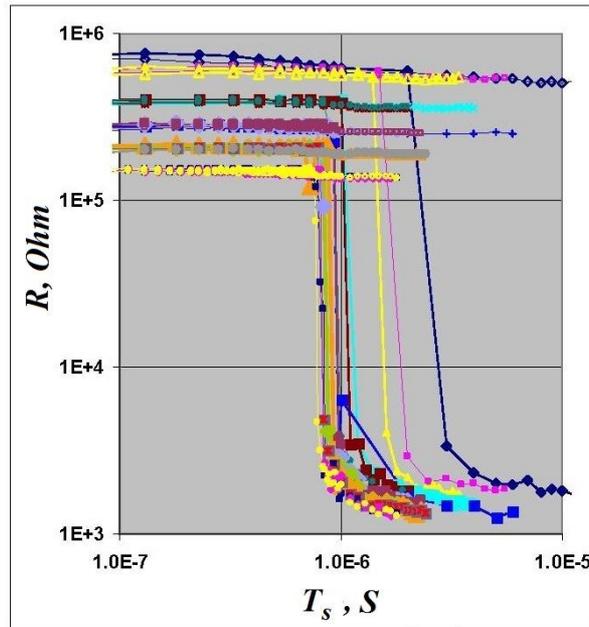
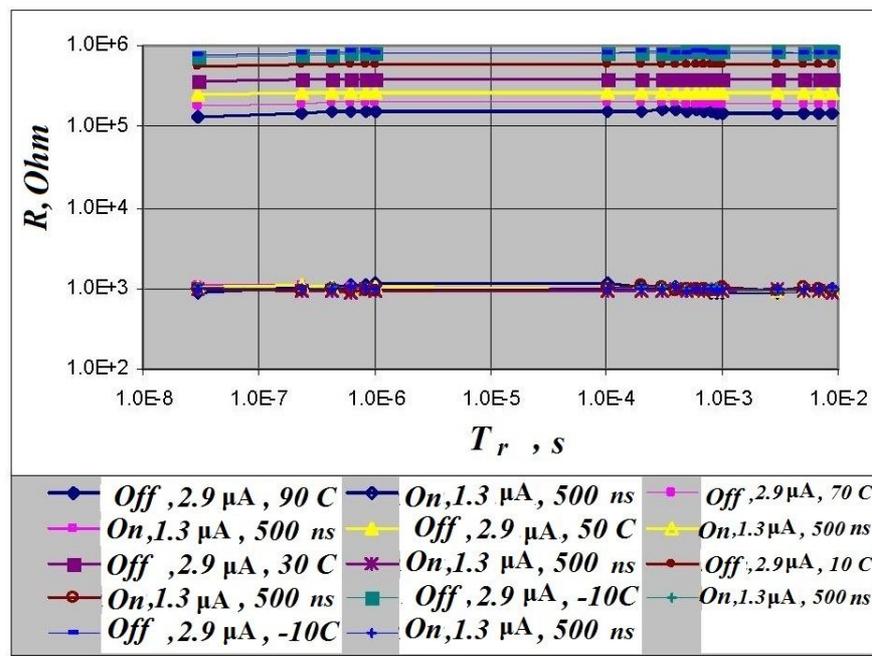
Alloy	Lower electric contact (LEC)	Upper electric contact (UEC)	T_s (for $I r_a$), c	T_s (for $1.2 I r_a$), c	On-speed: $I r_{min} / I r_a * 20$ ns
№225 CC BDL	C	C	3e-7	3e-6	0.4
№225 FF LS	TiAlN 2 mOhm cm	TiW	3e-7	2.8e-6	2.7
№225 FF BDL	TiAlN 5 mOhm cm	Ti-TiN-Ti	3e-8	7e-8	1.2
LRA FF BDL	TiAlN 5 mOhm cm	Ti-TiN-Ti	1.5e-8	4e-8	1.35
HPC FF BDL	TiAlN-C	Ti-TiN-Ti	2e-8	4e-8	1.1
LRA EBL	C	C-MoN	4e-8	5e-8	1.2
LRA EBL	MoN	C-MoN	5e-8	2e-7	1.5

where №225 is the alloy $Ge_2Sb_2Te_5$, CC – carbon contacts, FF – metal contacts, LS – lateral switching of CGS state XCII, BDL – electric breakdown layer of CGS, LRA – low-resistance alloy of CGS, EBL – electron-beam lithography.

From the above data we can draw the following *conclusions*. Transition to a lower-resistance alloy improves the on-speed, especially for $1.2 I r_a$. Material and resistance of the lower contact have less influence on the on-speed. Addition of Ti-layer to the upper contact improves considerably the on-speed. This is probably due to the fact that the inclusion of Ti-layer into the alloy film of GST № 225 provides a good ohmic contact. Off-speed depends little on the modifications of the upper contact, but depends on the conductivity of the lower contact and CGS alloy. Conductivity of CGS, produced using EBL, is higher and, therefore, the off-speed of NVM increases, even with the application of carbon contacts.

Temperature dependence of the programming speed. Off- resistance changes with the temperature because generation of current carriers in CGS is an active process. Fig. 8 shows different initial off-levels. As on-pulse duration increases with temperature reduction, each of the corresponding RT curves drops to the on-level. Duration of the pulse, necessary for reaching a definite off-resistance level, reduces as temperature increases, i.e. on-speed of the device increases [3].

Let us make some *conclusions*: (R_s -dU/dI), I_s and I_r are practically not dependent on temperature; growth of the programming resistance is accompanied by a continuous growth of activation energy; T_s reduces as temperature increases, i.e. with the growth of activation energy in the range from 0.05 to 0.3 eV (Fig. 8); for the device with carbon contacts of CC type, T_r does not depend the temperature in the range of 20 ns – 10 ms (Fig. 9).


 Fig. 8. Dependence of the on-speed, T_s , on the temperature

 Fig. 9. T_r dependence in the temperature range of 10 – 90 °C for GST device № 225 CC BDL

Material of the electrodes. Let us demonstrate that carbon contacts are unique in their application as electrode materials. An advantage of carbon is change of its resistance from a relatively resistive material to the high-conductivity material, but only in the close vicinity to CGS contact zone. Heating, when current is passed through C-SiNx-C stack, causes certain changes. In this case SiNx acts as an electric breakdown layer that localizes the device operation to the close vicinity of the breakdown region [3]. Fig. 10 shows that when current passes through the device its conductivity gradually increases. Initially, resistance of the device is about 1E6 Ohm, then, when electric signal with the current of 2 mA and voltage of 3V is supplied, electric breakdown occurs. After that the device changes its resistance to 1E4 Ohm. Further growth of the current causes gradual reduction of the device resistance from 1E3 Ohm to 100 Ohm.

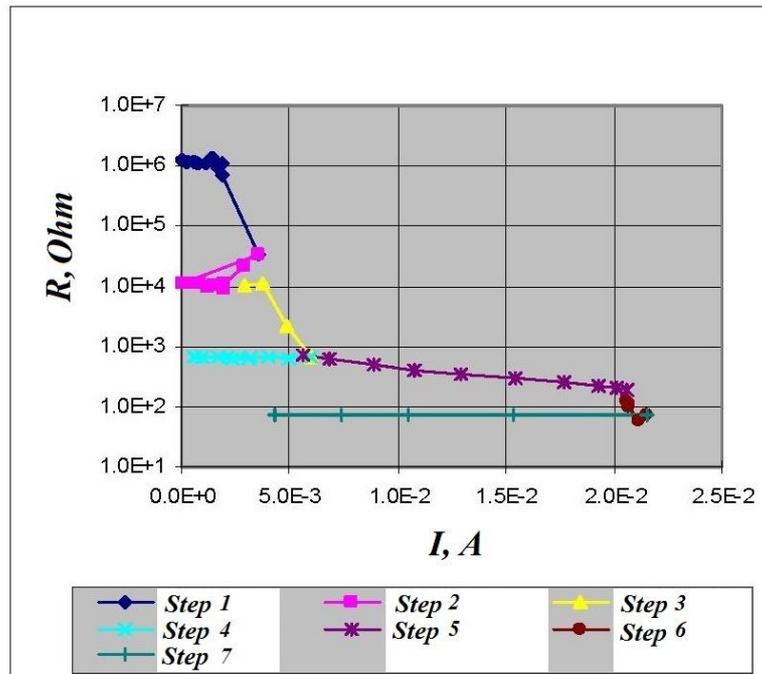


Fig. 10. Electric formation of the cell C-SiNx-C

Heating of such devices at the temperature of 350 ° C during 72 hours does not cause further changes. If the device is switched off, heating at the temperature below 350° C does not lead to higher conductivity [3]. The results are entered to Table 2.

Table 2

Thermal treatment results

Resistance before the moment of switching C-SiNx-C, Ohm	Resistance after application of electric pulses, Ohm	Resistance of the same devices after firing at the temperature of 350 ° C during 72 hours (slow cooling), Ohm
1.96e6	444	511
1.25e6	3.46e4	3.42e4
8.15e5	1.5e4	1.4e4
1.56e6	210	289
2.7e6	814	886
1.7e6	Without switching	1.3e5
1.2e6	Without switching	9.1e4
1.4e6	Without switching	9.4e4
9.6e5	Without switching	8.5e4

Thus, we can make a conclusion that a carbon contact is formed in the close vicinity of the breakdown zone where programming temperature reaches 650 – 700 ° C. This provides the advantage of isotropic heat conductivity, in which heat conductivity, perpendicular to the area of the device, is considerably higher than that at the lateral side and enables effective thermal isolation of the device. This experiment makes it possible to suggest that carbon contacts change the resistance only along the current path and remain more electrically and thermally resistive when deviations from the current path occur. Hence, lateral heat losses through the contact thickness are minimized. NVM of BDL type, where the lower contact is made from carbon, is switched faster than that with TiAlN. However, it should be noted that off-speed could increase if the lower contact if the lower contact uses TiAlN alloy with higher resistance value.

Conclusions

Threshold off-resistance value Rr_0 of NVM changes proportionally to CGS film thickness. For resistance of the device R_{CGS} at low electric field such dependence is not confirmed, although crystallization front of the material spreads from the cathode to anode along the current path. The experiments show that crystalline regions of the phase-change alloy GST № 225 are virtual contacts to the upper interface of the electrode (the anode), which leads to a faster switching of MC phase states. Therefore, on-speed does not depend on the cathode contact but depends essentially on the anode contact. If the anode coupling with CGS material is made weaker, i.e. less resistive, on-speed will increase. The anode material selection is made taking into account conductivity of the alloy of CGS, directly adjacent to it, in order to minimize low-field resistance of the interface. Experiments show that NVM off-speed with lower resistance of the contact material is mainly determined by the heat loss through the lower contact (the cathode) and the adjacent regions of CGS film. So off-speed (of overwriting, reset) can depend strongly on the cathode contact (both on its material and geometry), but to be insensitive to changes in the anode contact. This indicates the presence of the polarity of the current flow through MC. Therefore, a higher NVM off-speed can be achieved by minimizing side heat losses at the cathode. Amorphous carbon has a property of changing the resistance only in the direction of current flow, so the use of amorphous carbon as the cathode material is optimal.

REFERENCES

1. Ovshinsky S. R. Reversible electrical switching phenomena in disordered structures / S. R. Ovshinsky // Physical Review Letters. – 1968. – № 21. – P. 1450 – 1453.
2. Phase Change Memory / H.-S. Philip Wong [et al.] // Proceedings of the IEEE. – 2010. – Vol. 98, №. 12. – P. 2201 – 2227.
3. Phase change memory technology [Електронний ресурс] / Vipin Rajendran [et al.] / IBM Research. – 2009. Режим доступу: http://www.itrs.net/ITWG/Beyond_CMOS/2010Memory_April/Proponent/Nanowire%20PCRAM.pdf.
4. Костылев С. Электронное переключение в аморфных полупроводниках / С. Костылев, В. Шкут. – Наукова думка: Київ, 1978. – с. 203.

Slobodian Ivan – Junior lecturer of the Department of Telecommunication Systems and Television. Vinnytsia National Technical University.