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DIGITAL RECEIVER ON THE BASE OF PLIC

There had been presented theoretical and experimental research of digital receiver on the base of DSP signal processor, the possibility of construction the receiver with digital processing is shown. It is suggested to use one of the classes of signal processors, algorithm for receiver operation has been elaborated.

***Key words**: digital receiver, signal processor DSP, arithmetic and logic unit, filtration, digital signal.*

Introduction with problem set-up

New direction of development of microelectronic digital and analog-to-digital element base and appearance of new components allow to elaborate high-quality receivers on the base of digital principles of radio signal processing [1].

Digital processing of signals in receiving systems can be applied from the sphere of radiopath, where signal frequency decreases to digitize the signal without losses applying ADC and then to process this signal by digital signal processor or specialized processor [2]

The objective of this paper is construction of digital receiver on the base of DSP signal processor.

Analysis of chosen method

Fig. 1 shows structural diagram of digital receiver, which uses modern technical solutions in the sphere of digital processing of the signal based on FT.

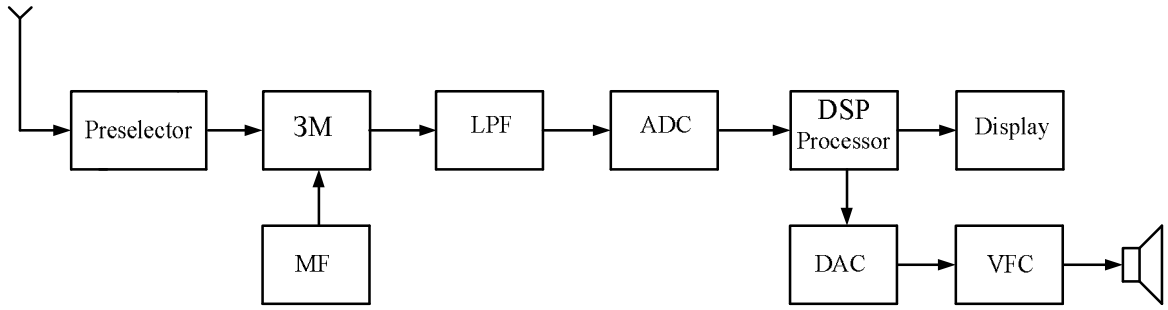

Fig. 1. Structural diagram of digital receiver

ADC transforms analog signal, received from the output of the wideband FT into digital flow of indications, and further processing is executed by digital methods.

The main elements of digital part of receiver are centered in the module of digital receiver. This module produces channel filtration and signal demodulation. The module can process one or several receiving channels. The main module components are high frequency ADC, digital quadrature step-down DDC converter and signal processor [3].

Information flow of demodulated data from one or several receiving channels passes from module output into the computation unit for further processing. Data from other analogous receiving modules connected to FT output of analog receiving tracks of other ranges, enter the same unit.

Method for realization of DSP signal processor and operation algorithm

DSP signal processors allow to perform high processing of the weakest level signals. In conjunction with using of automatic filtration the improvement of signal/noise ratio occurs and signal quality increases.

To realize digital receiver on the base of digital signal processor TMS320C2x microprocessor has been chosen. The receiver with high characteristics can be realized on the base of this processor. The processor will incorporate functions of control and radiosignal processing, namely high filtration and detecting.

The reason to chose this signal processor is that it is performed according to Harvard architecture, based on distribution of access buses to built-in memory of programs and data. It allows to execute the selection of instruction and data in one machine cycle and it provides execution of most instructions during one cycle. The processor contains a great number of built-in filters and the set of detectors, that allows to produce receivers of high quality.

Fig. 2 shows the structure of typical signal processor with fixed comma TMS320C2x.

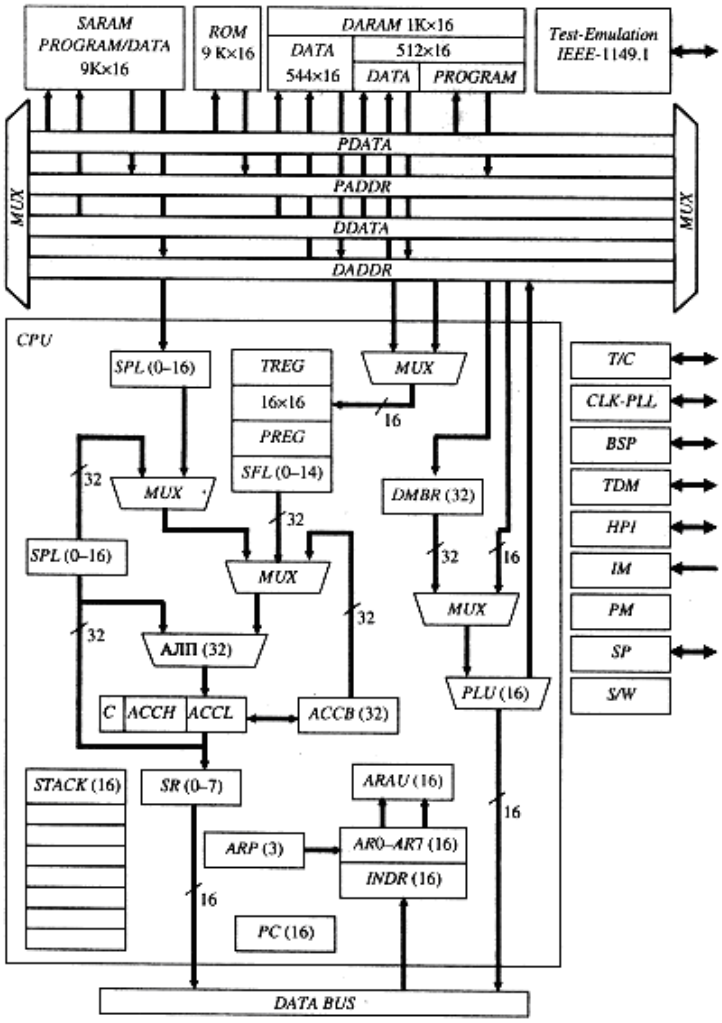

Fig. 2. Typical architecture of digital signal processor

TMS320C2x signal processor consists of central processor unit (CPU), built-in memory of programs and several functional peripheral devices, that allows to avoid using additional external devices [4].

Central processor unit, CPU. It consists of:

32-bit ALU, it executes most instructions during one cycle;

storage cell ACC, divided in two segments by 16 bits (ACCH i ACCL);

accumulator buffer ACCB;

arithmetic device of auxiliary registers ARA U;

register file AR0-AR7 and register INDR;

independent logical unit PLU;

hardware multiplier 16x16;

commands indicator PC;

multiplexers MUX.

Arithmetic logic unit (ALU). Data from one of such units enter the first input of ALU: scaling and shift register SPL; SFL shift register at the output of PREG register of PREG multiplier and accumulator buffer ACCB.

At the second ALU input data are always sent by ACC storage cell and operation result is also sent to ACC . Shift register, SR, connected with ACC output performs left shift on 0-7 digits, that is executed in the cycle of data transfer from ALU on internal data bus.

Hardware multiplier 16x16. It performs all operations on numbers with and without sign. Operands arrive from data memory. One of the operands can be constant, directly sent in the instruction. To save temporary one of the operands 16-bit TREG register is used. Multiplication result is downloaded in 32-bit PREG register.

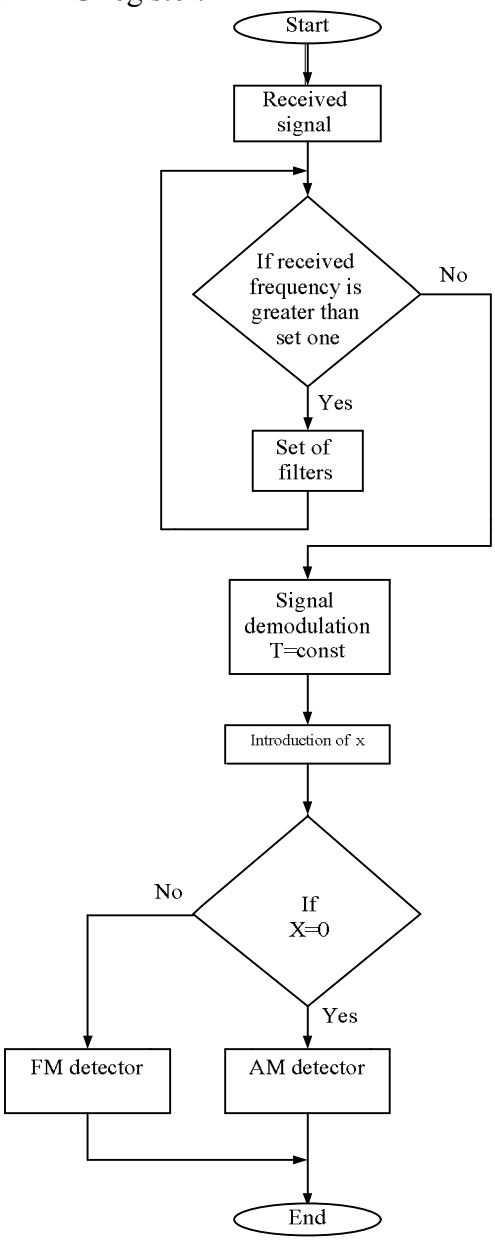

Fig. 3. Algorithm of digital receiver operation

Logic unit PLU executes operation independently on ALU, the result of operations in PLU does not influence on bits of ALU state. The first operand arrives to PLU from data memory, the second – from memory or programs of bits manipulation register DBMR. Specific logical instructions

executed only by PLU, allow in 16-bit word to install and clear any quantity of bits in random combination. The result of operations in PLU is stored in the same data storage cell, where the first operand was chosen from. Thus, logic operations can be performed with the content of any data storage cell, in particular with the content of the first 16 input/output ports, that can be addressed as data memory (50H-5FH address).

For normal operation of the receiver, it is necessary to adjust correctly its components. As soon as they are adjusted, the receiver must respond to changes of signal level and control elements.

Fig. 3 presents the algorithm of digital receiver operation, implemented on signal processor.

The results of simulation

DSPhilrus program for digital filtration was applied for experimental research. 22 buttons of ready filters are allocated in the left part of the window of this program. To study AFC and characteristics of each of these filters it is sufficient to press the button of the required filter and then the button "Хар" – in the window we will see the enlarged AFC and detailed characteristics of the chosen filter.

Band pass filters are used for SSB-signal detection under conditions when other SSB-signal is precisely allocated on the frequency of useful signal. The advantages are based on the fact that the energy of SSB-signal is not distributed uniformly but depending on peculiarities of specific voice, is concentrated in relatively narrow spectral region. In case of successful selection of band pass filter parameters (coincidence of its AFC maximums with regions, where great part of energy of useful SSB-signal is concentrated), signal/noise ratio can be improved.

Fig. 4 shows weak SSB-signal in noises at turned- off DSPhilrus

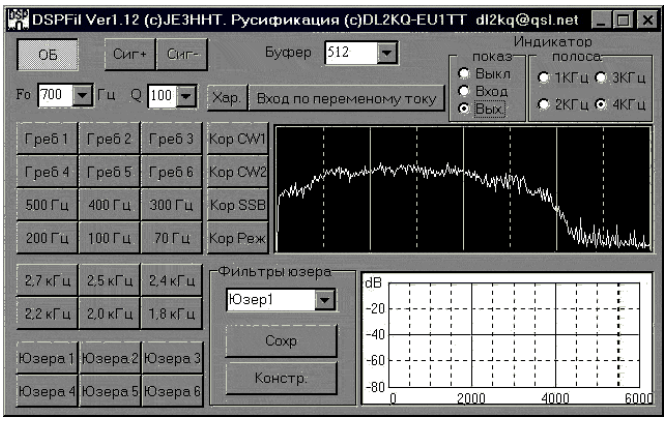

Fig. 4. Weak SSB-signal in noises at turned- off DSPhilrus

Let us connect the band pass filter 2,2 kHz and we will obtain the following result.

Fig. 5 shows SSB-signal during connection of band pass filter 2,2 kHz.

Fig. 5. SSB-signal while connection of band pass filter 2,2 kHz

Fig. 6 shows SSB-signal during connection of “Uzer 4” filter

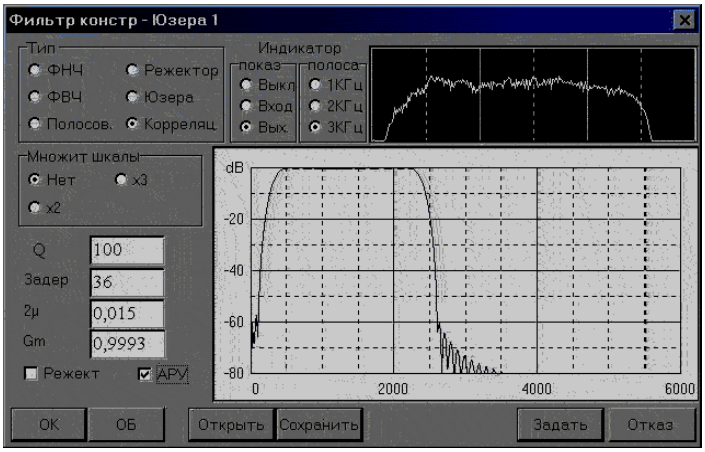

Fig. 6. SSB-signal while connection of “Uzer 4” filter

The window below on the left shows the AFC, of the filter, connected at this moment filter. AFC of the designed filter, appears only after clicking "OK." In the window "Type" we set the type of designed filter.

Conclusions

Digital receiver on the base of digital signal processor, that provides high characteristics of the device was synthesized. Realization of DSP signal processor and algorithm of its operation was suggested. Experimental research were carried out, as a result quality filtered SSB-signal was obtained. The obtained results are of great importance for practical application in designing of new radio receiving devices or modernization of existing ones.

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