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O. D. Azarov, Dc. Sc. (Eng.), Prof.; M. Yu. Shabatura; O. G. Murashchenko

SECOND-TYPE DYNAMIC ERRORS IN FAST-ACTING SUCCESSIVE APPROXIMATION ADC WITH WEIGHT REDUNDANCY

The paper considers mathematical models of the second-type dynamic errors occurring in a fast-acting successive approximation analog-to-digital converter with weight redundancy. Response speed values for a fast-acting successive approximation ADC converter with weight redundancy are found for second-type errors compensation. Such conversion is shown to be possible for different forms of input signal level change.

Kew-words: *analog-to-digital converter, dynamic errors, weight redundancy, modeling, numbering system, successive balancing.*

Introduction

ADC is an indispensable component of modern informational measuring systems [5] as well as modern systems of analog and digital signals processing. Successive approximation ADC occupies a significant place among different classes of information converters. At the same time it should be noted that successive approximation ADC are traditionally built using binary numbering systems, which causes considerable dynamic errors in the case of input signal level being changed in the course of transformation. For solving the above-mentioned problem, analog signal sampling-and-storage device is traditionally used at the input of such ADC for fixing while input signal level is being converted. However, this causes several-time increase of a conversion error.

The problem of dynamic errors compensation in successive approximation ADC was investigated in the USA [5] and USSR, particularly, in Vinnytsia Polytechnic Institute (today – Vinnytsia National Technical University) [1, 2, 3].

Current importance of the problem

Works [1, 4] proposed to use methods of ADC dynamic errors reduction. However, second-type dynamic errors were not discussed.

An approach is known for significant reduction of dynamic errors consisting in building successive approximation ADC based on the numbering system with weight redundancy. This makes it possible to trace changes of input signal level and, therefore, to reduce considerably the level of second-type dynamic errors. Besides, it should be mentioned that weight redundancy application enables compensation of considerable first-type dynamic errors. It should be also noted that complex application of the first and second approaches enables considerable increase of the frequency range of converter signals [1].

In research papers [2, 4] this trend is not disclosed comprehensively and systematically. Thus, the subject of this paper, dealing with analysis of the second-type dynamic errors in successive approximation ADC with weight redundancy, can be considered actual.

Goal

Reduction of second-type dynamic errors in successive approximation ADC with weight redundancy.

Tasks

1) To consider the possibilities of reducing second-type dynamic errors that occur in binary successive approximation ADC while signals that change in time are being converted;

2) To consider the possibilities to simulate the process of compensating the dynamic errors that

appear in the process of fast successive balancing with weight redundancy.

Solution of the tasks

Numbering systems with weight redundancy (NSWR) are numbering systems (NS) that belong to the class of positional numbering systems.

Any numbering system must be represented by a basis and a base. In NSWR a natural basis is distinguished, i.e. a set of bit weights with the values formed as an increasing geometric progression of the numbers $\alpha^0, \alpha^1, \alpha^2, \ldots, \alpha^{n-1}$, where α is the base that is defined as the ratio of weights of two adjacent bits.

An example of natural basis:

$2^0, 2^1, 2^2, \ldots, 2^{n-1}$ – with the base α=2;

$10^0, 10^1, 10^2, \ldots, 10^{n-1}$ – with the base α=10 of the binary and decimal numbering systems correspondingly.

In the case of classical "golden proportion" $\alpha = \frac{1+\sqrt{5}}{2} \approx 1{,}618$ we have the basis consisting from a set of numbers: 1; 1,618; 2,618; 4,236; …; $1{,}618^{n-1}$.

Any integer number N in numbering systems with integer-valued α can be represented in the form of

$$N = \sum_{i=0}^{n-1} a_i \cdot \alpha^i , \qquad (1)$$

where i=0, 1, 2, …, n-1 – bit number; $a_i \in \{0,1\}; \{\overline{1},1\}; \{\overline{1},0,1\}$ – binary digit in the i-th bit or an alphabet; α=1; 2; …; 10 – bases of the numerical system; α^i – weight of the i-th bit; (n-1) – number of the higher-order bit.

If base α is an irrational number, i.e. a "golden" p or S proportion [2], then a real number can be represented in the form of:

$$D = \sum_{i=-\infty}^{n-1} a_i \cdot \alpha^i . \qquad (3)$$

Any natural number is represented in the form of

$$N = \sum_{i=-n}^{n-1} a_i \cdot \alpha_p^i , \qquad (4)$$

where $\alpha_p^i = \alpha_p^{i-1} + \alpha_p^{i-p-1}$ – the i-th power of golden proportion.

Method error ΔN of number imaging depends on the set of alphabet a_i. If $a_i \in \{0,1\}$, then $\Delta N \le 1{,}0$, and such system is NSWR (0, 1). If $a_i \in \{\overline{1},1\}, \Delta N \le 2{,}0$, we have NSWR ($\overline{1}$, 1). If $a_i \in \{\overline{1},0,1\}$ $\Delta N \le 1{,}0$, the system is called NSWR($\overline{1}$, 0, 1).

In numbering systems with artificial basis the weights of bits are formed as sequences of integer numbers:

$$\varphi^0, \varphi^1, \varphi^2, \ldots, \varphi^{n-1} . \qquad (5)$$

Connection between the weight of the i-th bit is formed as a definite sum of lower-order bits:

$$\varphi_i = \varphi_{i-1} + \varphi_{i-2} + \ldots + \varphi_{i-k} . \qquad (6)$$

p-numbers of Fibonacci [1], Kotz numbers and others can serve as examples of such sequences.

Representation of integer numbers in the numbering systems with artificial basis looks like:

$$N = \sum_{i=0}^{n-1} a_i \cdot \varphi_i , \tag{7}$$

where a_i – bit coefficient in the i-th bit; i – bit number; φ_i – weight of the i-th bit that is an integer number.

Conversion ranges are determined for different numbering systems.

For binary NS we have:

$$D_2(n) = 2^n - 1, \tag{8}$$

where n – chosen number of bits.

For NSWR :

$$D_\alpha(n_\alpha) = \alpha^{n_\alpha} - 1, \tag{9}$$

where $n\alpha$ – number of NSWR bits under the condition of ranges similarity.

Along with multiformity of number representation in NSWR, NS data are distinguished by the following: the sum of weights of lower-order bits exceeds the weight of the current higher-order bit:

$$\sum_{0}^{i-1} Q_j - Q_i > 0 \cdot \tag{10}$$

NSWR is characterized both by an absolute weight redundancy coefficient in the form of

$$\Delta Q_i = \sum_{0}^{i-1} Q_j - Q_i \tag{11}$$

and by a relative weight redundancy coefficient:

$$\delta Q = \frac{\sum_{0}^{i-1} Q_j - Q_i}{\sum_{0}^{i} Q_j}. \tag{12}$$

For NSWR-based ADC efficiency evaluation fig. 1 is used.

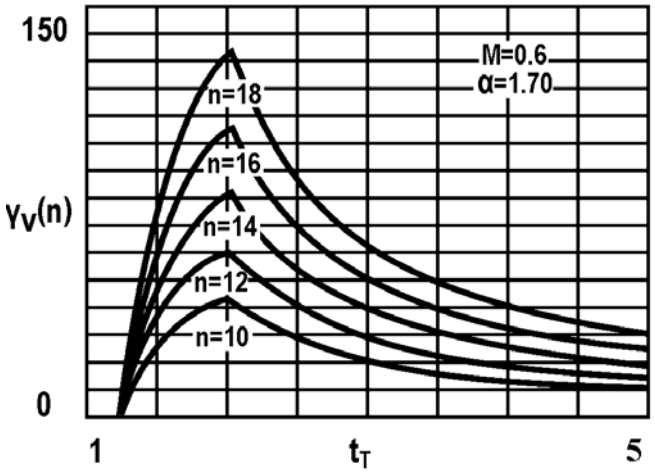

Fig.1. Functional dependence of the efficiency on the bit capacity n for α =1,7, scaling multiplier M=0,6 in ADC

When both non-redundant NS (NNS) and NSWR are used, conversion of analog signals into their digital equivalents is accompanied by a number of static and dynamic errors.

The mechanism of second-type dynamic error occurrence [9] in binary ADC is connected with the change of the level of input signal $A_{вх}$ in the course of conversion. This paper considers different

variants of a signal change at the input of successive ADC using NSWR and NNS.

Signal change at ADC input can cause the appearance of the second-type error – $\Delta''_{дин}$ that depends on the type of analog-to-digital conversion. In this case successive balancing is used as the most efficient one.

$\Delta''_{дин}$ is the speed of the input signal change that can be represented as the voltage or current time variation.

The compensating signal (it compensates the input signal) is expressed by [1]:

$$A_{k_n}(t) = a_n Q_n - a_n Q_n e^{-t_t/T}, \tag{13}$$

where $a \in (1,-1)$ – bit coefficients of the code, Q_n – weight of the converter bit; $^{-}t_t$ – balancing cycle duration; T – time constant of the transient process.

The corresponding part of $-a_n Q_n e^{-t_t/T}$ [1] is mathematical description of the first-type dynamic error that depends on the inertia of the converter analog units and has considerable influence on the second-type dynamic error.

For dynamic errors evaluation in successive balancing ADC using different NSWR as well as NNS, application of the single-type mathematical models of these errors in the form of balance equations will be expedient

For linear variation of $A_{вх}$ balance equation has the form of

$$F(\Delta A_{вх}, x, \alpha, n) = 0, \tag{14}$$

where $\Delta A_{вх}$ – input signal variation, a – base of the numbering system; x – unknown quantity for calculations; n – number of bits.

For non-inertial balancing in the case of increasing $A_{вх}$, initial expression for balance equation $F(\Delta A_v, \alpha) = 0$ has the form of:

$$\Delta A_{кв} = 2\Delta A_v^+ + Q_1 - Q_0, \tag{15}$$

where ΔA_v – $A_{вх}$ change within one cycle.

On the basis of the last relationship $\Delta A_{v\,\max}^+ = \dfrac{2{,}5 - \alpha}{2}$.

Total change of the input signal $A_{вх}$ is defined by the expression:

$$A_{вх}(t) = A_{вх.n}(t) + \Delta A_{вх}(t), \tag{16}$$

where $\Delta A_{вх}(t)$ – change of the input signal within the whole balancing period; $A_{вх.n}(t)$ – input signal value before balancing.

For the signal that is increasing or decreasing linearly $\Delta A_{вх}(t)$ can be expressed by:

$$\Delta A_{вх}(t) = \pm \Delta A_v t / t_T, \tag{17}$$

where $\pm\Delta A_v$ – change of $A_{вх}$ within one cycle; t – balancing time; t_T – duration of the conversion cycle.

For the signal that is increasing or decreasing exponentially $\Delta A_{вх}(t)$ can be expressed by:

$$\Delta A_{вх}(t) = \pm \Delta A_c * e^{-t/\tau}, \tag{18}$$

where τ – time constant of the input signal establishment; $\pm\Delta A_c$ – amplitude of $A_{вх}$ jump before balancing starts; t – conversion time.

Special software is developed that enables adequate analysis and investigation of the second-type dynamic errors in ADC of successive approximation [7]. In all of the figures given below input signal is depicted in black and compensating signal – in red color.

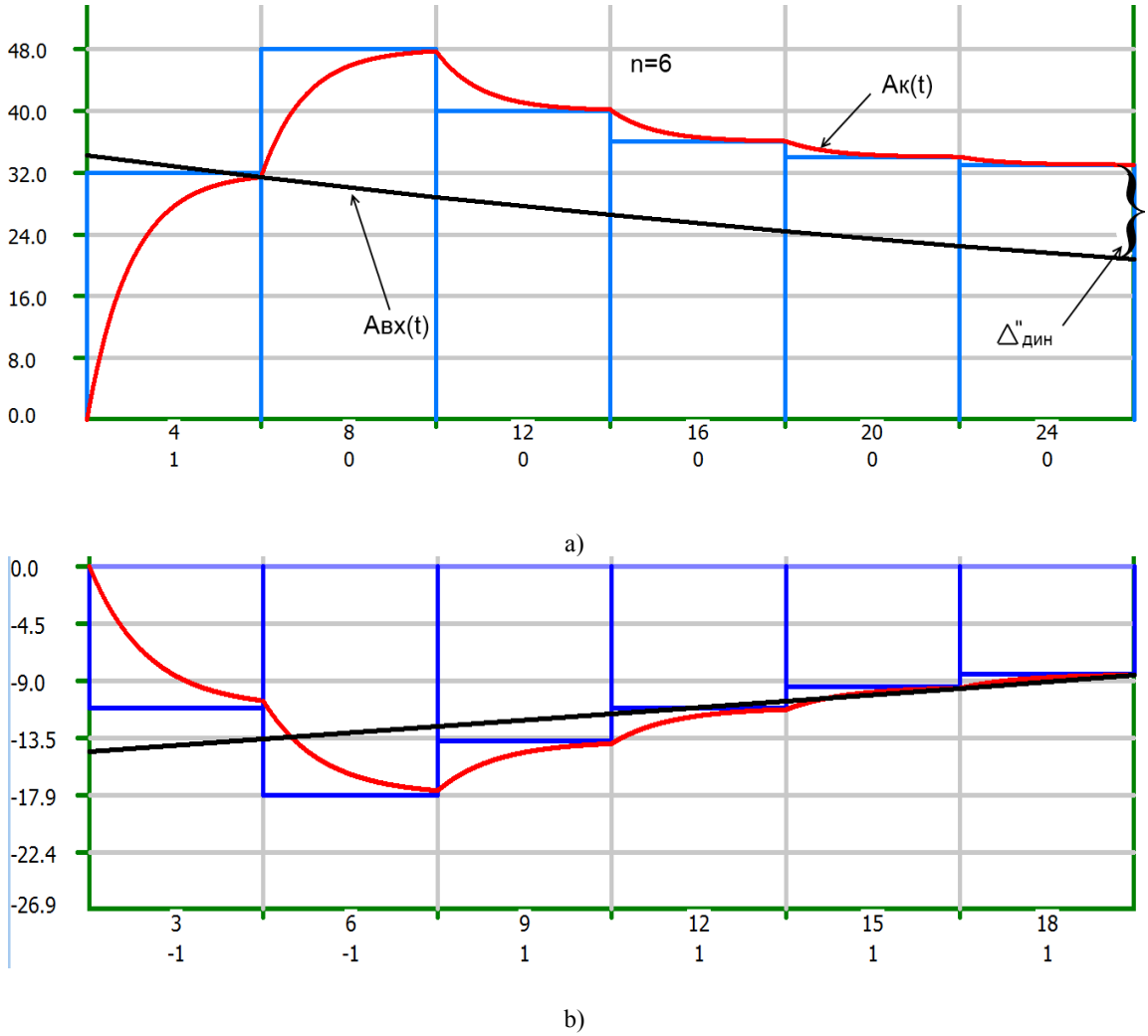

Fig. 2. Diagram of the successively balanced input signal: a) $A_{вх}$ is falling in binary ADC; b) $A_{вх}$ is increasing in ADC with weight redundancy

In fig. 2 $\Delta''_{дин}$ can be seen clearly between input and output signals in a binary 6-bit successive approximation ADC.

Now we shall discuss results of the research on second-type dynamic errors compensation in the successive balancing ADC with weight redundancy. Numbering system base – 1,618.

In fig. 2 b) relative deviation of the compensating signal from the input one for linear growth of the input signal using NSWR: Δ =2,1. When binary numbering system is used in ADC with successive balancing, relative deviation of the compensating signal from the input one is : Δ = 33.

According to the successive balancing diagram shown in fig 2 b), initial expression for the balance equation Fi(x,α,n)=0 is given by the relationship

$$\Delta Q_5 = \sum_1^3 Q_i - Q_4 - \Delta Q_i^* + 2,5Q_0 , \qquad (19)$$

where ΔQ_i^* – function from the establishment error that appears in the previous cycles $\Delta Q_1^* = xQ_1 + x\Delta Q_2^*$.

Similarly, for other errors: $\Delta Q_2^* = xQ_2 + x\Delta Q_3^*$, …, $\Delta Q_4^* = xQ_4 + x\Delta Q_5^*$

Relative deviation of the compensating signal from the input one for exponential decrease using NSWR: $\Delta = 2{,}4$. When binary numbering system is used in successive balancing ADC, relative deviation of the compensating signal from the input one is: $\Delta = 12$.

$\Delta A_{вх}$ for exponential signal may exceed significantly ΔA_{v} level for linear signal in successive balancing ADC with weight redundancy. At the lower-order balancing cycles changes of $A_{вх}$ that increases and decreases exponentially cannot exceed ΔA_{v}.

This condition is given by the relationship:

$$\Delta A_{вхм}^{**} = m\Delta A_v, \tag{20}$$

where $\Delta A_v = \Delta A_{вх}^{**} e^{-(n-m-2)t_T/\tau_c}$ – "residual" amplitude $\Delta A_{вх}$ before the beginning of m last balancing cycles.

In this case time constant of the input exponential signal cannot exceed the value of [2]:

$$\tau_c \le \frac{(n-m-2)t_T}{\ln\dfrac{\Delta A_{вх}^{**}}{m\Delta A_v}}. \tag{21}$$

If this condition is satisfied, accurate balancing of the input signal that increases or decreases exponentially is ensured, its initial amplitude not exceeding $\Delta A_{вх}^{**}$.

Significantly higher values of relative deviation of the compensating signal when input signal level is changed can be seen and compared in fig. 2 that shows diagrams of successive balancing in 16-bit ADC and in ADC with weight redundancy correspondingly.

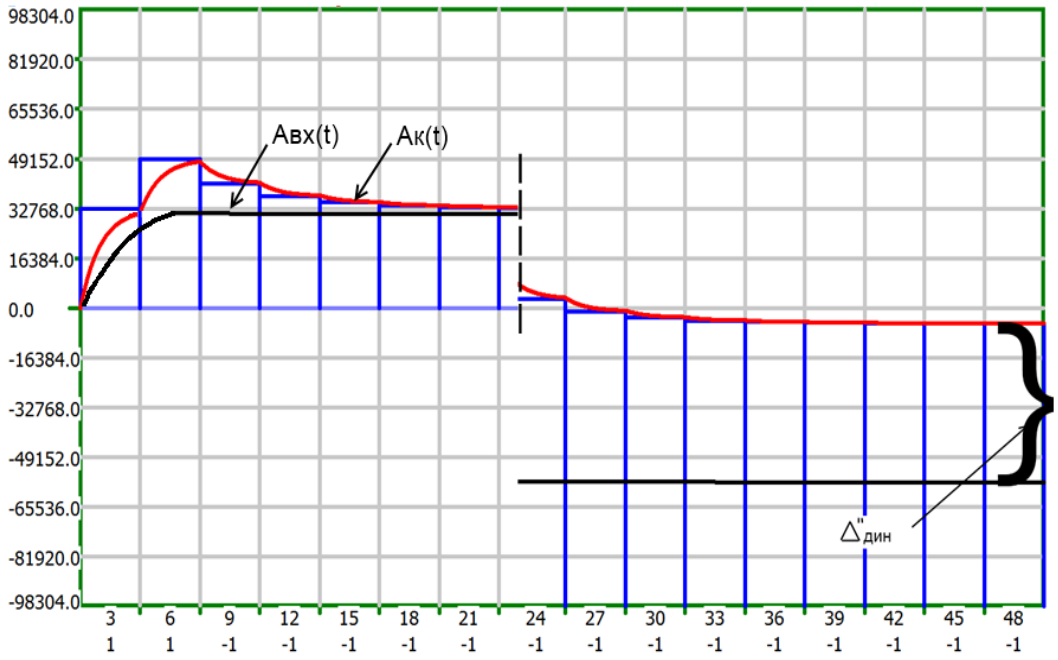

Fig. 4. Diagram of sucesive balancing of the input signal that decreases exponentially in 16-bit binary ADC

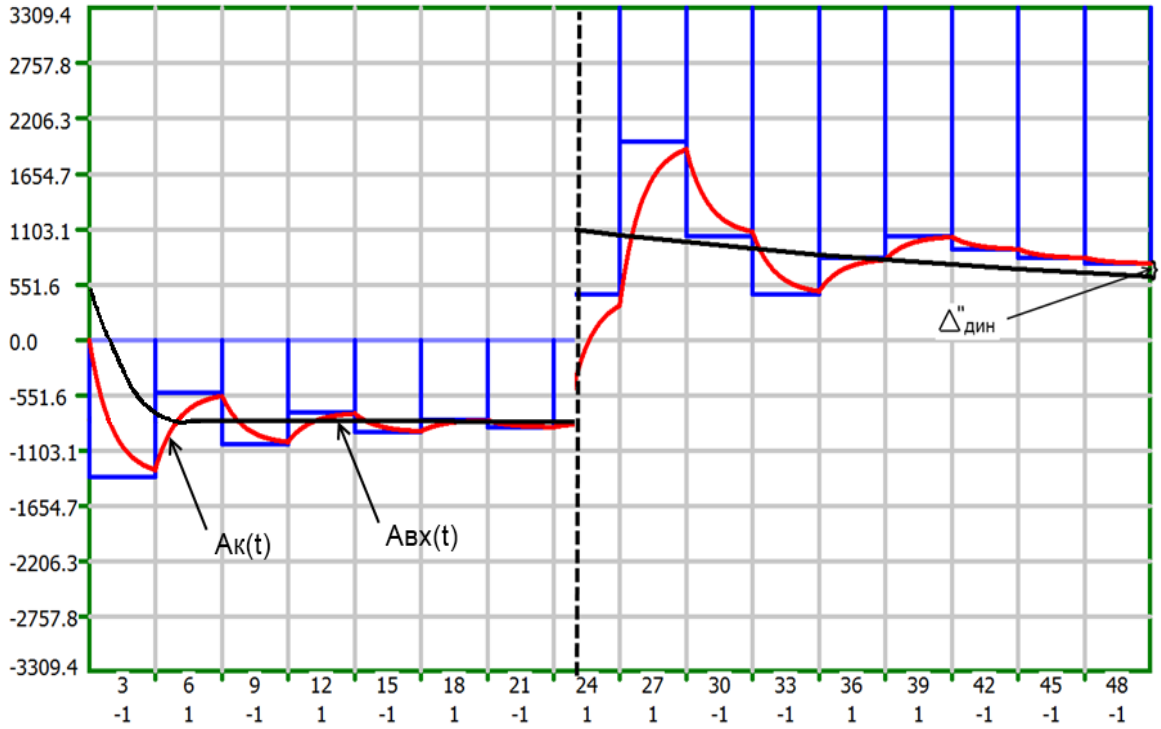

Fig. 5. Diagram of sucessive balancing of the input signal that decreases exponentially in 16-bit ADC with weight redundancy

According to fig. 4 relative deviation of the compensating signal from the input one in a binary system: $\Delta = 1666{,}2$. According to fig. 5, if NSWR is introduced into ADC of successive balancing, relative deviation of the compensating signal from the input one is: $\Delta = 2{,}9$.

In the process of ADC bits commutation, when analog compensating signal Ak(t) is being formed, different forms of transient processes could occur, e.g. presence of a feedback amplifier in the input signals comparator circuit [3] may cause oscillation processes in the output reaction if step inputs are observed [8]. Irrespective of concrete implementation of an amplifier comparative circuit, differences ΔA are designed so that its transient response would correspond to the first- or second-order circuit functions. In the first variant exponential transient process is observed.

The elaborated mathematical model of second-type dynamic errors compensation in successive approximation ADC makes it possible to convert input signals into their digital equivalents directly at a definite stage of the oscillation process caused by the feedback amplifier. This gives an extremely fast conversion speed along with its accuracy as compared with an ordinary binary ADC that is “waiting” for a complete “fading” of the oscillation process.

Hence, we see that gain in the dynamic error compensation in ADC of bitwise balancing is much higher due to NSWR application in such ADC. Besides, with the increase of bit capacity in the converter with weight redundancy second-type dynamic error compensation is also increased considerably as compared to the converter where binary numbering system or other NNS are used.

Conclusions

1. Mathematical models of second-type dynamic errors in successive balancing ADC have been elaborated.

2. It is shown that second-type dynamic errors of successive ADC can be compensated by weight redundancy introduction. This enables considerable increase of ADC speed as well as significant acceleration in balancing of the increasing or decreasing of both linear and exponential input signals.

3. It is demonstrated that response speed of successive balancing ADC with weight redundancy can be evaluated already at the design stage using computer simulation.

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Olexiy Azarov – Dc. Sc. (Eng.), prof., director of the Institute of Information Technologies and Computer Engineering, head of the chair of Computation Engineering.

Maxim Shabatura – Master's course student of the chair of Computational Engineering, the Institute of Information Technologies and Computer Engineering. E-mail – smydev@gmail.com, tel. 0977535830. Vinnytsia National Technical University.

Olexandr Murashchenko – project manager of "Liana" company.