V. M. Kychak, Dc. Sc. (Eng.), Prof., D. V. Myhalevskyy, O. V. Krypskyy

NOISE MODEL OF FET FOR FORECASTING THEIR RELIABILITY ON LEVEL OF LF NOISE

The paper analysis internal noises of FET and suggests noise model, considering the scheme of switching. There had been researched the dependences of noise voltage of FET on the operation mode as well as determined the tolerance ranges of noise voltage within which the FET is reliable.

Key words: *reliability forecasting, FET, mean-square noise voltage, LF noise, electronic devices.*

Introduction

Increase in integration level of unipolar integral schemes due to decrease in threshold voltage and consumption capacity causes the necessity in improvement technological methods of manufacturing of electronic engineering products (EEP), which improve quality of these devices. Availability of physical and chemical drawbacks in initial semi-conducting materials and other factors, causes fluctuation in the failures rate within wide range, with further screening non-reliable parts on the stage of initial control on manufacturing enterprise and input control as for meeting technical characteristics on enterprises assembling electronic devices [1, 2]. The above actualizes the development of methods and means for controlling over reliability of EEP on the stage of manufacturing and incoming inspection, which would allow to improve the reliability of EEP.

The first stage during the development of new method of reliability forecasting as for LF noise is choosing the optimal noise model, reflecting noise process in semiconductor, which depend on faulty sections of the structure. Paper [3] analyzed and researched the nature of noise of 1/f type for MTS-transistors, built following the CMOS technology with different type of conductivity. The objective of this work is to develop the optimum noise model for wide spectrum of FET for creation of new methods of forecasting their reliability.

Task setting

The set objective requires analysis of all the sources of own noises and determine optimal conditions and modes for measuring the informative parameters, ensuring the highest reliability for revealing potentially unreliable EEP.

Using noise model, requires to conduct researches dependences of noise parameters and characteristics of FET on the operation mode, and to determine the allowed limits of noise voltage, within which FET will be potentially reliable.

Noise model of FET

FETs, depending on operation principles and manufacturing technologies, may be divided into 2 types [4]. The first type of transistors is characterized by bulk channel of conductivity, which is the section of homogeneous semiconductor, separated from drain region and source by the united layer, which is formed with the help of p-n barrier. The second type unites transistors with surface channel of conductivity, which is formed by inverse layers under influence of under influence of external electric field and is the metal-dielectric semiconductor (MDS) structure.

Noise models for both structures will be similar, the difference is in mechanism of appearance LF noises in the channel. Considering [5], model of transistor for analysis of noise characteristic is shown on fig. 1.

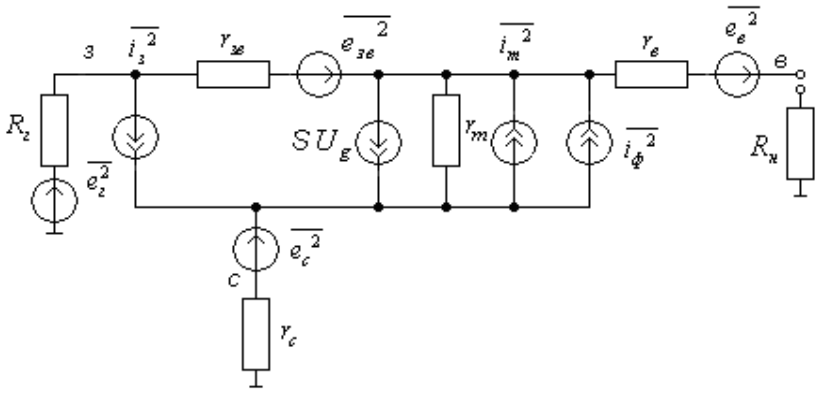


Fig. 1. Noise model of FET

The model uses the noise generator on the input $\overline{e_c^2}$. For analysis, we assume that all noise sources are independent . the main source of heat noise is frequency independent current generator $\overline{i_m^2}$ which is described by Nyquist formula.

$$\overline{i_m^2} = 4kTr_m S_{\max}^2 \Delta f \ ,$$

where $S_{\max}$ − slope of transistor saturation.

On the spurious elements of sink, source and of transistor, there appear sources of heat current:

$$\overline{e_в^2} = 4kTr_в \Delta f \ ,$$

$$\overline{e_c^2} = 4kTr_c \Delta f \ ,$$

$$\overline{e_{зв}^2} = 4kTr_{зв} \Delta f \ .$$

Current generator $\overline{i_з^2}$ is characterized by short noise of transistor which depends on direct reverse current and is determined by the expression:

$$\overline{i_з^2} = 2qI_{зв} \Delta f \ ,$$

where $I_{зв}$ − direct reverse current of transistor.

Noises the expressions for which are given above, are true for both types of FETs. Noises, level of which increases with decreasing of frequency are typical for low-frequency bands. In transistors with p-n-barriers this type of noise appears in the result of fluctuations, which take place in the metallic channel. These fluctuations, in turn, appear in the result of processes of generation – recombination on defective centers of channel and depleted section of p-n-barrier. For this type of transistors it is possible to determine low-frequency constituent from the expression:

$$\overline{i_f^2} = 4kT\Delta f S_{\max}^2 \left(\frac{p_1}{f} + \frac{p_2}{1 + f / f_0} \right),$$

where p_1, p_2, f_0 − coefficients of internal structure of transistor, which depend on material and temperature low-frequency constituent of noise of MIS transistor appears in the result of random capture of charge carrier by surface defects of sections which verge on semiconductor – dielectric of the metallic channel. The value of such type of noise may be determined by the expression.

The second constituent LF noise of MIS transistors – noise of generation – recombination, which appears in combined layer of support. It may be determined by the formula:

$$\overline{i_{f1}^2} = 4kT\Delta f S_{\max}^2 \frac{p_1}{f}.$$

The second constituent LF noise of MDS transistors – noise of generation – recombination, which appears in combined layer of support. It may be determined by the formula:

$$\overline{i_{f2}^2} = 4kT\Delta f S_{max.к}^2 \left(\frac{p_2}{f} + \frac{p_3}{1 + f / f_0} \right),$$

where $S_{\max.к}^2$ – slope of current control in channel by voltage on support;

p_2, p_3, f_0 – coefficients, which depend on noise of combination-recombination.

Considering [5], general root-mean-square value of noise voltage and noise current for model, showed on fig.1, may be written as follows:

$$\overline{e^2} = \frac{\overline{i_f^2}}{S_{max}^2} + \frac{\overline{i_m^2}}{S_{max}^2} + \overline{e_{зв}^2} + \overline{e_c^2} + \overline{e_в^2} \frac{R_{in}^2 (1 + r_m S_{max})^2}{r_в^2 r_m^2 S_{max}^2}, \quad (1)$$

$$\overline{i^2} = \frac{\overline{i_f^2}}{R_{in}^2 S_{max}^2} + \frac{\overline{i_m^2}}{R_{in}^2 S_{max}^2} + \overline{i_з^2}. \quad (2)$$

Consequently, the above expressions allow to make a decision that the level of own low frequency noise characteristics for MOS transistors increases the level of own noises of transistors with p-n-barrier. This is conditioned by availability of noise of generation-recombination in MDS structures.

Noise model with consideration of switching circuit

Transistor's internal parameters are usually considered during mathematical simulation of noise characteristics of transistors. The results of calculations are of approximate character, therefore they do not coincide with the experiment on practice. This may come true for transistors with high level of own noises. Low noise transistors, on the contrary, have the constituents of heat noise of switching circuit elements and feed back on the input of measuring devise, which causes measuring errors.

As is known [6], switching circuit for measuring noise ensures optimal operation mode from the point of view of maximum noise voltage. Therefore it is appropriate to consider all the types of noise constituents, which are entered by the circuit. During further calculations we will consider the MIS structure of transistor as the mostly spread one, which considers the switching circuit. The general noise picture of transistor under research may be shown in fig. 2

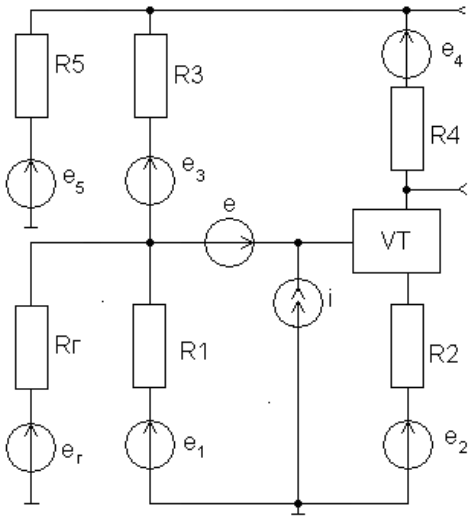


Fig. 2. Noise model of transistor switching

Each source of noise which acts in the circuit, is an independent one , therefore the source of noise voltage $\overline{e_1}$, $\overline{e_2}$, $\overline{e_3}$, $\overline{e_4}$, $\overline{e_5}$, $\overline{e_г}$ will be the sources of heat noise of corresponding resistors, and sources $\overline{e}$, $\overline{i}$ are determined by equivalent values of noise voltage and current (formulas 1, 2). Let us determine the constituents for each noise generator (fig.2) which influence the general noise voltage on the output of the circuit under research. Thus, for the noise generator on the input it is possible to write

$$\overline{U_г^2} = \overline{e_г^2}\left(\frac{R4R5^2R1}{\left(\frac{R4R5R1}{(R4+R5)\left(\frac{R4R5}{R4+R5}+R1\right)}+Rг\right)\left(\frac{R4R5}{R4+R5}+R3\right)}\right)^2.$$

Noise constituent due to potential divider:

$$\overline{U_1^2} = \overline{e_1^2}\left(\frac{\left(\frac{R4R5}{R4+R5}+R3\right)R_г R4R5}{\left(\frac{R4R5}{R4+R5}+R3+R_г\right)(R4+R5)\left(R4Rг\frac{\frac{R4R5}{R4+R5}+R3}{\frac{R4R5}{R4+R5}+R3+Rг}+R1\right)}\right)^2,$$

$$\overline{U_3^2} = \overline{e_3^2}\left(\frac{R4R5}{\left(\frac{R4R5}{R4+R5}+R3+\frac{R_\text{г}R1}{R_\text{г}+R1}\right)(R4+R5)}\right)^2.$$

For the resistor of blocking filter, the noise constituents is

$$\overline{U_5^2} = \overline{e_5^2}\left(\frac{\left(R3+\frac{R_\text{г}R1}{R_\text{г}+R1}\right)R4}{\left(R5+\frac{\left(R3+\frac{R_\text{г}R1}{R_\text{г}+R1}\right)R4}{R3+R4+\frac{R_\text{г}R1}{R_\text{г}+R1}}\right)\left(R3+R4+\frac{R_\text{г}R1}{R_\text{г}+R1}\right)}\right)^2.$$

The noise constituent of voltage of source resistance may be determined by the expression:

$$\overline{U_4^2} = \overline{e_4^2}\left(\frac{\left(R5+R3+\frac{R_\text{г}R1}{R_\text{г}+R1}\right)R4}{\left(R3+\frac{R_\text{г}R1}{R_\text{г}+R1}\right)R5+R4\left(R3+R5+\frac{R_\text{г}R1}{R_\text{г}+R1}\right)}\right)^2.$$

Constituent of source of equivalent noise voltage due to internal noises of transistor on the circuit output may be written as

$$\overline{U_e^2} = \overline{e^2}\left(\frac{\big(R3(R4+R5)+R5(R3+R4)\big)R4(R3+R4+R5)}{R5R3(R3+R4)(R4+R5)}\right)^2.$$

Constituent of noise voltage may be determined as

$$\overline{U_i^2} = \overline{i^2}\left(\frac{\left(R3+\frac{R4R5}{R4+R5}\right)(R5+R4)}{R5}\right)^2.$$

Noise sources are uncorrelated, therefore the law of superposition, considering which the total noise voltage on the output of switching circuit may be determined as:

$$\overline{U_ш^2} = \overline{U_1^2}+\overline{U_2^2}+\overline{U_3^2}+\overline{U_4^2}+\overline{U_5^2}+\overline{U_e^2}+\overline{U_i^2}+\overline{U_\text{г}^2}. \quad (3)$$

Substituting the above constituents into the expression (3) and considering the mode of short circuit on the input , we receive:

$$\overline{U_ш^2} = C^2\overline{e^2}+\frac{\overline{e_3^2}R4^2}{A^2}+\overline{e_5^2}\left(\frac{R4R3}{(R5+B)(R3+R4)}\right)^2+\overline{e_4^2}\left(\frac{(R5+R3)R4}{R3R5+R4(R3+R5)}\right)^2+\overline{i^2}A^2, \quad (4)$$

where $A = \dfrac{\left(R3 + \dfrac{R4R5}{R4+R5}\right)(R5+R4)}{R5}$, $B = \dfrac{R4R3}{R4+R3}$,

$C = \dfrac{\big(R3(R4+R5)+R5(R3+R4)\big)R4(R3+R4+R5)}{R5R3(R3+R4)(R4+R5)}$.

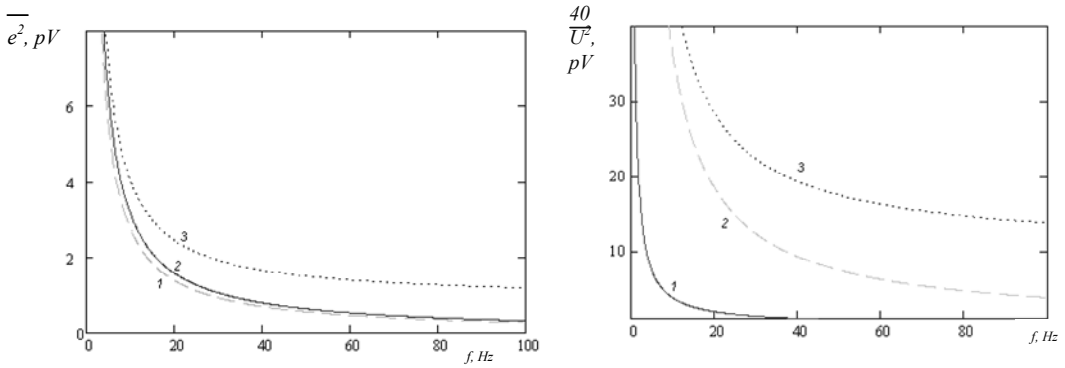
Considering the expressions (1) and (2) and grouping the corresponding sources of noise, the expression (4) may be re-written:

$$U_{ш} = 4kT\Delta f\left(C^2 r_m + C^2 r_{зв} + C^2 r_c + \frac{C^2 R_{вх}^2 (1 + r_m S_{\max})^2}{r_в^2 r_m^2 S_{\max}^2} + \frac{R5R3^2 R4^2}{(R5+B)^2 (R3+R4)^2} \right) +$$

$$+ 4kT\Delta f\left(R4\left(\frac{(R5+R3)R4}{R3R5 + R4(R3+R5)} \right)^2 + \frac{r_m}{R_{вх}^2} A^2 + \frac{R4^2 R3}{A^2} \right) + 2qI_{зв} A^2 \Delta f +$$

$$+ 4kT\Delta f\left(S_{\max}^2 \frac{p_1}{f} + S_{\max.к}^2 \left(\frac{p_2}{f} + \frac{p_3}{1 + f/f_0} \right) \right)\left(\frac{C^2}{S_{\max}^2} + \frac{A^2}{S_{\max}^2 R_{вх}^2} \right).$$

The above expressions allow to evaluate the level of own noises in MIS transistors, considering operation mode, as well as a partial case and transistors with p-n-barrier, Using expressions (1) and (4), there had been conducted the research of dependance of roof-mean-square voltage on frequency (fig.3)



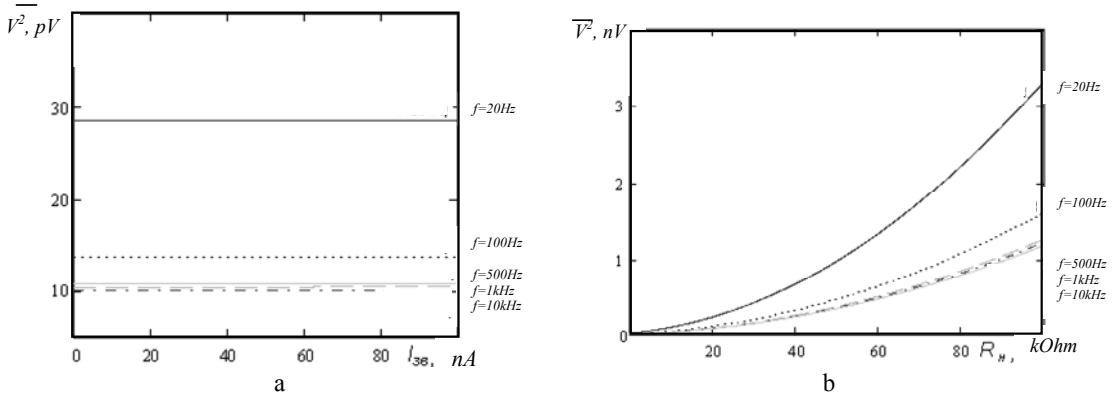
a b

Fig. 3. Dependence of noise voltage on frequency

As is seen from fig.3a, the lowest noise level is peculiar to transistors with insulated p-n-barrier (curve1). For MIS transistors it is seen that the highest noise level is peculiar to structures with high resistance support, which is explained by noise of generation-recombination, and for structures with low resistance-level of noises (curve 2) coincides with curve1. For transistors with high resistance support , the influence of LF noise is seen up to the frequency 100 KHz and above it.

Analysis of calculations, giver in fig 3b, shows that the dependence of roof-mean-square noise voltage on frequency, considering the influence of switching circuit elements, is of the same character, however, level of noise voltage differs by the order in comparison with the previous case, which may result in error during reliability forecast. Thus, it is necessary to consider the influence of heat noises of the circuit elements during forecast the reliability of FET.

There had been researched the influence of operation modes upon the level of roof-mean-square value of noise voltage on different frequencies, considering the elements of circuit (fig.4).



a b

Fig. 4. Dependence of noise voltage on gate current (a) and load resistance (b)

Fig. 4a presents the dependence of root-mean-square noise voltage on value of gate current. As was foreseen, the highest level of noise voltage takes place on frequency of 20 Hz, and it does not depend on current value. Changing loading resistance (fig. 4b), the dependence acquires non-linear character, and on frequency of 20 Hz – the highest slope. Thus, measurement of noise voltage requires to choose load resistance of switching circuit of FET which has the value of about 1 kOhm. The characteristics are non-linear around this point.

Conclusions

In the result of the researches there had been suggested the improved noise model for wide spectrum of EET with insulated p-n barrier MDS transistors, considering all noise sources of technological operations of reliability prediction.

Research results helped prove that the root-mean-square value of noise voltage of circuit differs by an order from the equivalent noise voltage of internal sources of transistor.

The results of the research of noise characteristics enable to make a conclusions that reliability forecast of different types of EEP has to be conducted of frequency of about 20 Hz. Exceeding noise level of transistors under research by one and half times of its calculating values allows to consider it as unreliable one.

REFERENCES

1. Горлов М.И., Андреев А.В., Ануфриев Л,П., Емельянов В.А. Технологические методы повышения надежности ИС в процессе серийного производства // Микроэлектроника. 2004. Том 33. №1. С. 24-34.

2. Горлов М.И., Андреев А.В. Входной контроль полупроводниковых изделий // Микроэлектроника. 2003. Том 32. №5. С. 390-399.

3. Степаненко И.П. Основы микроэлектроники. – М.: ЛБЗ, 2004. – 488 с.

4. Жигальский Г. П., Гваськов А. А., Ситкин П. О. Шум вида 1/f в транзисторах со структурой металл-диэлектрик-полупроводник с разным типом проводимости канала и топологическими размерами // Радиотехника и электроника. 2007. Том 52. № 6. С. 751-756.

5. Жалуд В., Кулешов В. Н. Шумы в полупроводниковых устройствах. Под ред. А. К. Нарышкина. Совместное советско-чешское издание. – М.: Советское радио. 1977. – 416 с.

6. Пряников В. С. Прогнозирование отказов полупроводниковых приборов. – М.: Энергия, 1978. – 112 с.

Kychak Vasyl – Doctor of Technical Sciences, Head of Department of Telecommunication Systems and Television.

Myhalvskyy Dmytro – Post graduate student with Department of Telecommunication Systems

Krypskyy Oleg – Post graduate student with Department of Telecommunication Systems

Vinnytsia National Technical University.