S. M. Saharchenko, Cand. Sc. (Eng)., Assist. Prof.

STRUCTURES OF INTEGRAL CAPACITORS AS THE BASIS FOR BUILDING CAPACITORS' MATRIXES FOR ADS WITH CHARGE REDISTRIBUTION WITH WEIGHT REDUNDANCY

There had been analyzed the contemporary methods for realization of integral capacitors. There had been suggested the capacitor structures for building capacitors' matrixes in the structure of ADC with charge redistribution.

Key words: *capacitor matrix, weight redundancy, lateral capacitor, integrated capacitor structures.*

ADC with charge redistributions (CR) [1] takes central place among ADC of successive approximation of average and high accuracy. This is explained by number of advantages in comparison with other structural realizations, in particular, lower power consumption, simplified structural realization due to elements interconnection, possibility of full integral realization on MOS technologies, high operation speed and accuracy. One of the perspective ways of further improvement of parameters of such devices is using weight redundancy [2]. This approach stipulates for changing ratio between the nominals of elements in capacitor matrix, which is the basic component of ADC with CR. Besides, retaining the resolving power of converter requires the extension of bit grid [3], that is, the number of matrix elements increase. The above results in increase in total capacity of ADC capacitor matrix with redundancy in comparison with traditional binary ones, which, in turn requires the increase in crystal area for placing additional capacitors during the usage of new structures of integral capacitors, which ensure high dencity of packing.

Thus, there is a task of choosing structural realization of integral capacitors and building capacitors' matrixes for ADC with CR with weight redundancy on its basis.

The solution of the set task requires:

- evaluation of degree of increase in capacity of capacitor matrix with weight redundancy in comparison with traditional binary ones;
- analysis of contemporary approaches for realization of integral capacitors and choose the most appropriate for this task;
- receiving mathematical correlation for calculating parameters of integral capacitors.

Matrix of weight type in the structure of ADC with CR is formed by capacitors with nominal values $C_0, C_0\alpha, C_0\alpha^2 ... C_0\alpha^{n-1}$, where C_0 – nominal value of capacitor with the lowest capacity, α – base of number system, n – number of discharges of convertor. The total volume of capacitor matrix will be determined as follows:

$$C_\Sigma = \sum_{i=0}^{n-1} C_0 \cdot \alpha^i = C_0 \cdot \frac{(\alpha^n - 1)}{\alpha - 1}. \quad (1)$$

Correct comparison of ADC with different calculating systems requires to consider the extension of bit grid, which is determined by an expression $\gamma = \ln 2 / \ln \alpha$ [3]. Thus, the total volume of capacitor matrix of ADC with weight redundancy, the resolution power of which makes up binary digits, will equal

$$C_{\Sigma\alpha} = C_0 \cdot \frac{(\alpha^k - 1)}{(\alpha - 1)}, \quad (2)$$

where $k = ceil(n \cdot \frac{\ln 2}{\ln \alpha})$, and function *ceil(x)* determines the results of rounding *x* upward to the nearest biggest integer, since the number of digits has to be the whole.

In this case the amplification factor of matrix capacity in the structure of ADC with weight

redundancy in comparison with the corresponding matrix of usual binomial convertor may be calculated as

$$\phi = \frac{C_{\Sigma\alpha}}{C_{\Sigma 2}} = \frac{(\alpha^k - 1)}{(2^n - 1)(\alpha - 1)}. \quad (3)$$

Graphic interpretation of the last expression for different values α and n is shown on fig. 1.

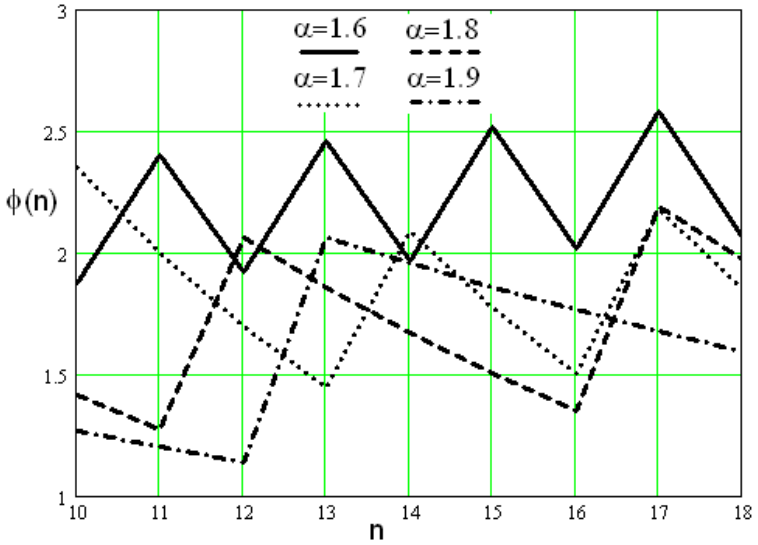


Fig. 1. Dependence of amplification factor of the integral capacity of ADC with RC on number of digits

The analysis of the latter shows that depending on basis of numerical system and number of digits the total capacity of matrix increases from 1,2 to 2,5 times, and in general case, the reduction of α increases the total capacity. Thus, it is necessary to choose the structural realization of integral capacitors, ensuring high density of package. Today thin film capacitors of different types are used for building capacitor matrixes in structure of ADC with CR. They differ by materials, used for manufacturing of electrodes and dielectric layer. The biggest linearity (0,01 %), but the worst density of package (1 fF/μm^2) is demonstrated by so-called metal-insulator-metal capacitors; a little worse linearity (0,1 %) with a little higher density is demonstrated by so-called poly-to-poly capacitors. As it follows from the name, in the first case the electrodes are thin metal plates, and in the second case-polycristal with corresponding admixtures. The most simple way of manufacturing insulator is using silicon (oxide capacitors), however it has low dielectric constant, and, consiquently, small capacity. Using composite dielectrics to increase the dielectric constant results in so-called oxide-nutride-oxide capacitors. There are dielectric materials, which are characterized by dielectric conductance on the level of some thousands; however the usage is not efficient from the point of view of economy.

From the point of view of realization of film capacitors, they may be divided into three categories: of vertical type (electrodes are located one over the other and are insulated by the layer of dielectric, fig. 2a), of horizontal type or lateral (electrodes are located close, fig. 2b), and of combined type (fig. 2c).

High density in package of vertical type capacitors is achieved by using multi–layer structure (HPP) and minimize the thickness of dielectric [4]. However, the density of package remains relatively small, apart from that, the creation of multi – layer capacitors requires additional steps of technological process, which increases the cost of these devices.

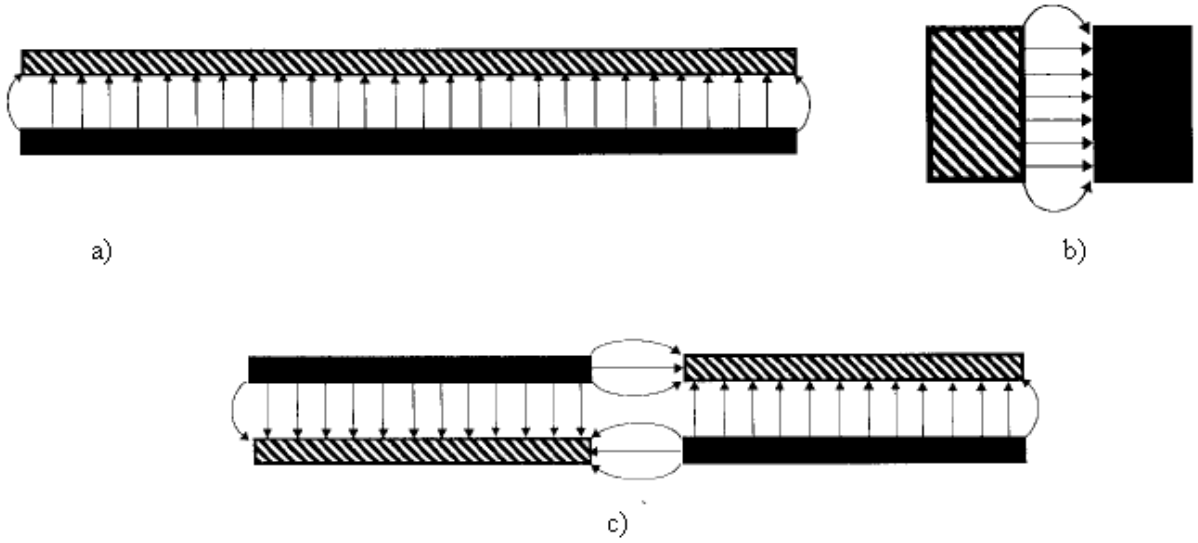


Fig. 2. Structures of film integral capacitors: a) of vertical type; b) of horizontal type; c) of combined type

The development of technology for manufacturing integral components, in particular, decreasing maximum distance between elements in one layer, enabled to create lateral capacitors, which are characterized by smaller distance between electrodes in comparison with vertical ones, where the distance between electrodes is determined by the thickness of oxide. In the results, the density of package on lateral capacitors under such conditions will be higher in comparison with usual vertical capacitors. The most famous structures in realization of lateral capacitors are inter-digital structure [5] and fractal structure [6].

The advantage of inter – digital structure is in the simplicity of its realization and relatively simple calculation of total capacity of capacitor in comparison with fractal one. This structure also allows to receive the set of capacitors with fixed correlation of nominals which is externally important for ADC with charge redistribution. The disadvantage is the increase in spurious inductance and decrease in total capacity in comparison with fractal one.

The multi-layer variants of lateral capacitors, in particular with structure of vertical parallel plates (VPP) – structure, fig. 3a) [7] and those with structure of vertical beams (VB – structure, fig. 3b) [7] are very popular today.

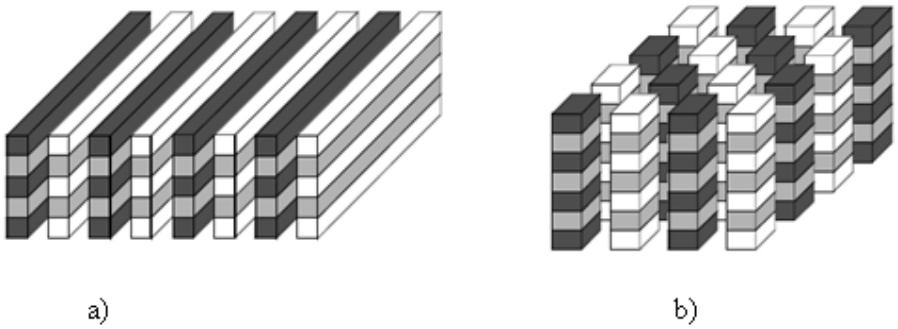


Fig. 3. Structure of multi layer integral capacitors: a) vertical parallel plates; b) vertical beams

Black and white colors represent layers which form the electrodes of capacitors, gray color – layer of interconnections. The simplicity of calculation of total capacity and simplicity of creation of massive of capacitors with the agreed nominals are peculiarities of structure of vertical parallel plates. Structure of vertical beams is characterized by big value of total capacity due to using the electric field on two axis.

Table 1 shows the results of experimental researches of different parameters of 3 the most

spread structural realization of integral capacitors with nominals of 1 and 10 pF [7]. Capacitors were made according to the following parameters of manufacturing process: minimum width and distance between topological elements was 0,24 μm, thickness, of oxide layer and metal layer was and t_{ox}=0.7 μm and t_{met}=0.53 μm, silicon oxide was used as dielectric, structures VPP and HPP were realized using 5 layers of metal, and VBB – 4 layers.

Table 1

Results of experimental researches of structures in integral capacitors

Structure	Average capacity C_0, pF	Square, μm^2	Capacitor constant, 1 GHz	Relative Deviation $\frac{\sigma_C}{C_0}$	Capacitive Density, aF/μm^2	Coefficient of improvement	Resonance Frequency, GHz
VPP	1.01	670	83.2	0.005	1512	7.4	>40
	11.46	7749	26.6	0.006	1480	8.0	11.3
VB	1.07	840	48.7	0.013	1281	6.3	37.1
	10.60	8666	17.8	0.007	1223	6.6	11.1
HPP	1.09	5378	63.8	0.024	203.6	1.0	21
	10.21	55615	23.5	0.0178	183.6	1.0	6.17

Analysis of table 1 shows that for the realization of precision capacitor matrixes, the lateral capacitors have advantages over traditional ones, and parameters VPP and VB structures are very close to each other. It also should be noted that VPP structures are characterized by maximum accuracy of manufacturing, which, independent of capacity of integral capacitor makes up apr. 0,5 %.

For using lateral capacitors during building of ADC with redistribution of charge, we consider the methods of calculation of their capacity under conditions of different parameters of technological process. Fig. 4a shows one of the possible realizations of VPP structures. Fig. 4b and 4c show the way the elementary capacitors are formed. It is obvious that the total capacity of such capacitor is determined as sum total nominals of elementary capacitor. Common capacitor is formed on the basis of two types of capacitors: $C_{vpp,x}$ та $C_{vpp,z}$. Capacity of capacitor $C_{vpp,x}$ may be calculated according to the formula:

$$C_{vpp,x} = \varepsilon_{ri} \cdot \varepsilon_0 \cdot \frac{A_y}{s}, \tag{4}$$

where ε_{ri} − dielectric constant of the dielectric between the components of the i-th layer, ε_0 − dielectric constant of vacuum, A_y − virtual square of electrodes, s − distance between components of the i-th layer.

Virtual square of electrodes is calculated according to the formula:

$$A_y = (L_y + w + \pi \cdot s/2) \cdot (t_м + t_д/2), \tag{5}$$

where L_y − length of the component, w − width of the component, $t_м$ − thickness of metal layer, $t_д$ − thickness of dielectric layer between neighboring metal layers.

It should be noted that virtual square of electrodes is somewhat bigger than the real one. This is explained by so-called fringing effect.

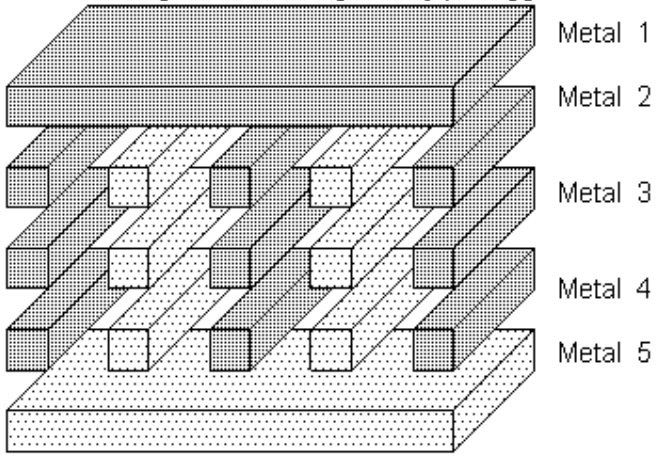
Capacity $C_{vpp,z}$: is calculated analogically:

$$C_{vpp,z} = \varepsilon_{rij} \cdot \varepsilon_0 \cdot \frac{(L_y + t_\partial/2) \cdot (w + s/2)}{t_\partial}, \quad (6)$$

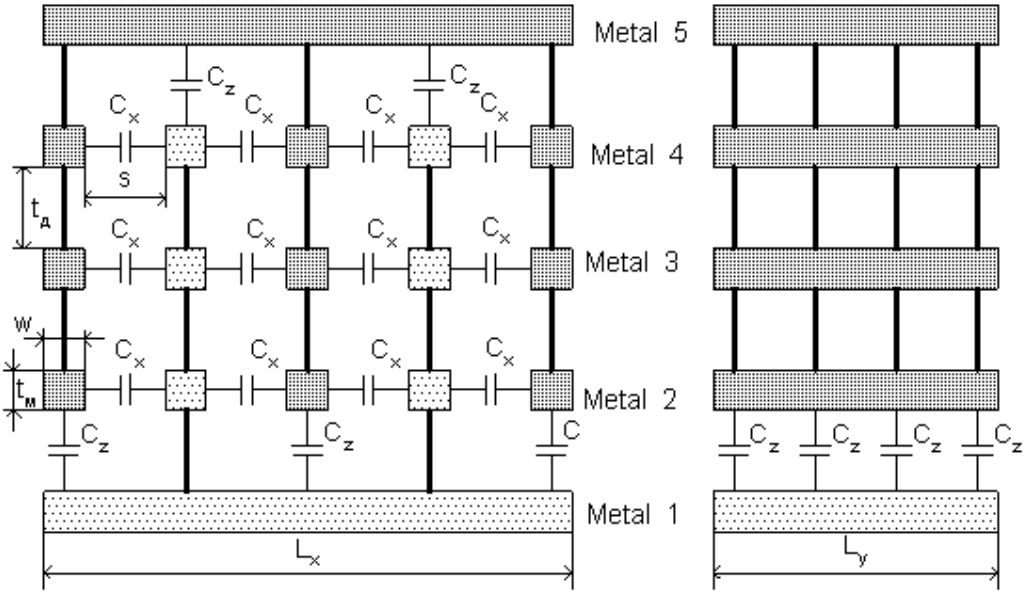
where ε_{rij} – dielectric constant of dielectric between the neighboring metal layers.
Total capacity may be calculated using the expression:

$$C_{vpp,з} = r \cdot C_{vpp,x} + l \cdot C_{vpp,z}, \quad (7)$$

where r and l number of capacitors correspondingly C vpp,x and C vpp,z.



a)



b) c)

Fig. 4. Structure of integral capacitor of VPP – type: a) three-D-view, б) front view, в) side view

In general case the last expression looks like:

$$C_{vpp,з} = Int(\frac{L_x - w}{w + s}) \cdot (n-2) \cdot C_{vpp,x} + (Int(\frac{L_x - w}{w + s}) + 1) \cdot C_{vpp,z}, \quad (8)$$

where *Int(a)* – whole part of expression *a*, L_x – width of integral capacitor, *n* – number of

metal layers.

Analogical way allows to receive the expression for calculation of the capacity of integral capacitor of VB-structure, common view of which is presented on fig.5a. Total capacity is determined as the sum total of capacities of elementary capacitors of three types: $C_{vb,x}, C_{vb,y}$ and $C_{vb,z}$ (fig. 5b − 5d). Capacity of each of them is determined by expression:

$$C_{vb,x} = \varepsilon_{ri} \cdot \varepsilon_0 \cdot \frac{(w_y + s_y/2) \cdot (t_м + t_д/2)}{s_x}, \tag{9}$$

$$C_{vb,y} = \varepsilon_{ri} \cdot \varepsilon_0 \cdot \frac{(w_x + s_x/2) \cdot (t_м + t_д/2)}{s_y}, \tag{10}$$

$$C_{vb,z} = \varepsilon_{rij} \cdot \varepsilon_0 \cdot \frac{(w_y + s_y/2) \cdot (w_x + s_x/2)}{t_д}. \tag{11}$$

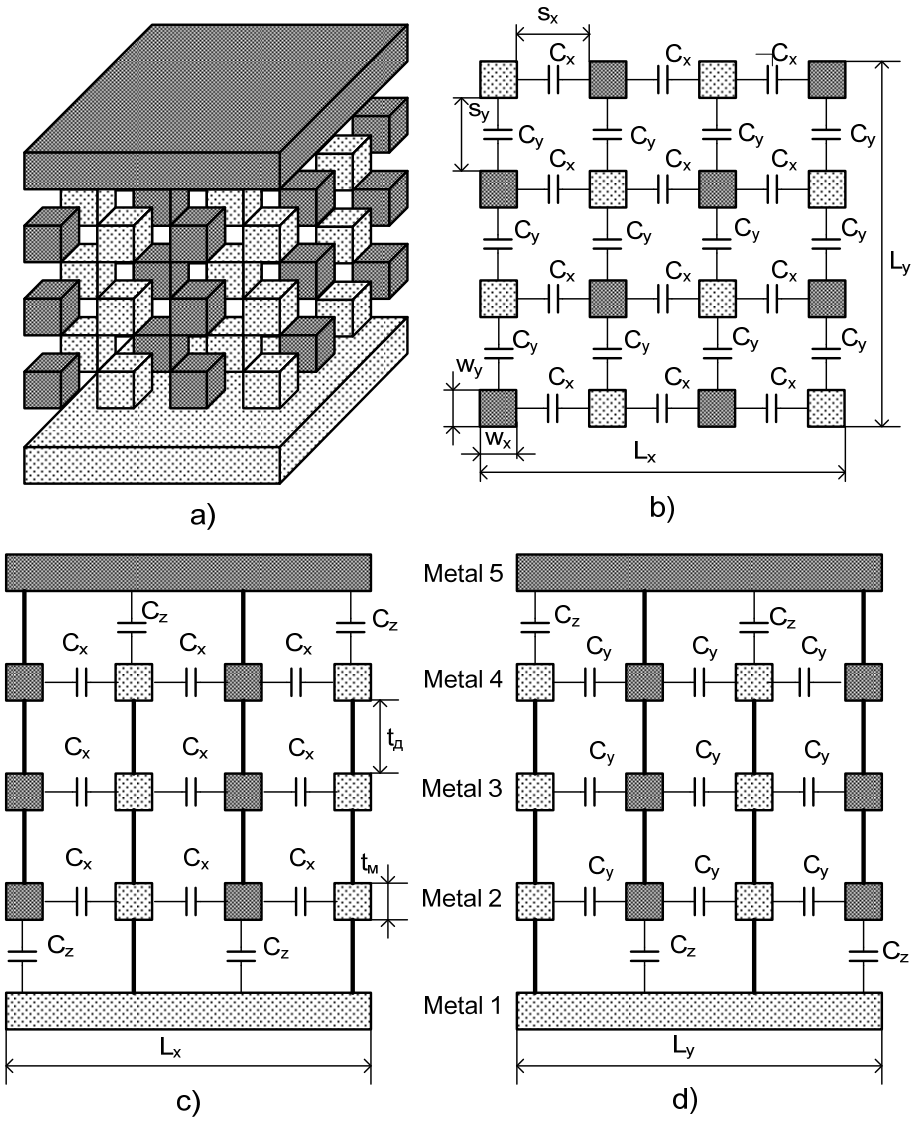


Fig. 5. Structure of integral capacitor of VB-type: a) three-D-view, b) top view (layers 1 and 5 are not shown), c) front view, d) side view

Assuming that $w_x=w_y=w$, $s_x=s_y=s$, the total capacity of such capacitor will equal

$$C_{vb,з} = Int(\frac{L_x - w}{w + s}) \cdot (Int(\frac{L_y - w}{w + s}) + 1) \cdot (n - 2) \cdot C_{vb,x} + ... \\ + Int(\frac{L_y - w}{w + s}) \cdot (Int(\frac{L_x - w}{w + s}) + 1) \cdot (n - 2) \cdot C_{vb,y} + (Int(\frac{L_x - w}{w + s}) + 1) \cdot (Int(\frac{L_y - w}{w + s}) + 1) \cdot C_{vb,z}. \quad (12)$$

Fig. 6 shows the dependence of capacity of integral capacitors of different types on number of mental layers.

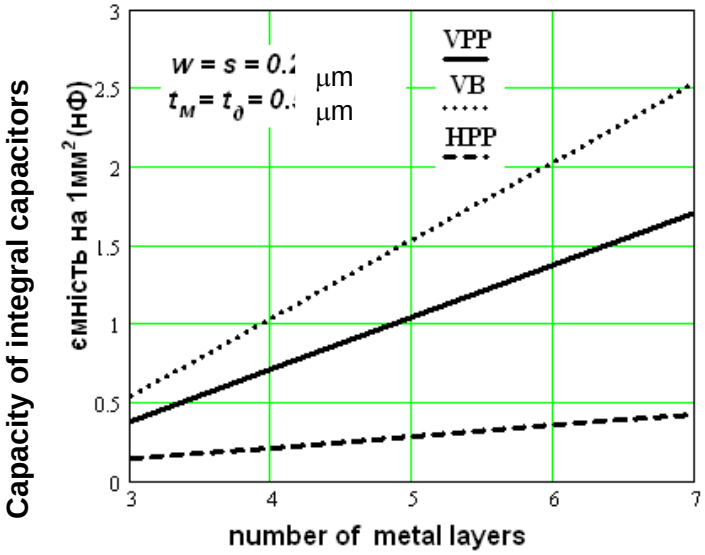


Fig. 6. Dependence of capacity of integral capacitors of different types on number of metal layers

Conclusions

The paper considers the modern approaches to the realization of integral capacitor structures with high density of package, analyses advantages and disadvantages of each of them for the realization of capacitor matrixes in the structure of ADC with CR. It had been shown that as for the aggregate of matrix factors of weight type, during the usage of weight redundancy it is expedient to realize in the kind of multy layers lateral structures of VB and VPP type.

REFERENCES

1. McCreary J. L., Gray P. R. All-MOS charge redistribution analog-to-digital conversion techniques. – Part 1 // IEEE J. Solid-State Circuits. – 1975. – Vol. 10. – P. 371 – 379.

2. Захарченко С. М., Азаров О. Д., Харьков О. М. Самокалібровані АЦП із накопиченням заряду на основі надлишкових позиційних систем числення. – Вінниця: УНІВЕРСУМ – Вінниця, 2005. – 235 с.

3. Азаров О.Д. Основи теорії аналого-цифрового перетворення на основі надлишкових позиційних систем числення. – Вінниця: УНІВЕРСУМ-Вінниця, 2004. – 260 с.

4. J. N. Burghartz. Integrated RF components in a SiGe bipolar technology / J. N. Burghartz, M. Soyuer, K. A. Jenkins, M. Kies, M. Dolan, K. J. Stein, J. Malinowski, D. L. Harame // IEEE Journal of Solid-State Circuits. – September 1997. – vol. 32. – P. 1440 - 1445.

5. Patent 5 208 725 USA, МПК H01J4/10, H01L27/02. High capacitance structures in a semiconductor device. / Akcasu O. E.; – №US005208725A; заявл. 19.08.92; опубл. 04.05.93.

6. H. Samavati, A. Hajimiri, A. R. Shahani, G. N. Nasserbakht, and T. H. Lee, "Fractal capacitors, "IEEE Journal of Solid-State Circuits, vol. 33, pp. 2035 - 2041, December 1998.

7. R. Aparicio and A. Hajimiri, "Capacity limits and matching properties of integrated capacitors, "IEEE Journal of Solid-State Circuits, vol. 37, pp. 384 - 393, March 2002.

Saharchenko Sergiy **–** Cand. Sc. (Eng.), Assistant Professor with the Department of Calculating Equipment.

Vinnytsia National Technical University.