**S. M. Zakharchenko, Sc. (Eng.), Assist. Prof.; O. V. Boiko**

# DEVELOPMENT AND RESEARCH OF DIGITAL CALIBRATION METHODS, USING WEIGHTS REDUNDANCY

*The paper presents the developed method of digital self-calibration of serial approximation ADC based on redundant positional systems of calculation, which enables to significantly reduce the methodological error of calibration and avoid the usage of additional digits.*

***Key words**: digital self-calibration A / D converter, analog-digital converter, weight redundancy, quantization error.*

Analog to digital converters are widely used in various devices and systems, in particular in data acquisition and processing, communication systems, various systems of technological control. Analog-to –digital converters with serial approximation (ADC SA) belong to such class of converters, which, on one hand, are of high accuracy, and , on the other hand are fast acting. These features concentrate the attention of specialists on these devices.

Problems, dealing with accuracy increase of ADC remain actual. Partially the problem of accuracy increase can be solved by improving the technology (the use of laser trimming of elements). However, this approach, besides substantial increase the cost of production, leads to further deterioration of the temperature parameters, reduces the reliability of devices. Another way to improve the accuracy characteristics of ADC SA is the application of self calibration methods. However, while using the binary system of calculation, calibration is carried out in digital-analog form, which provides the use of additional corrective DAC and reduces the speed of the converter.

To avoid the above-mentioned drawbacks, redundant positional system of calculation (RPCS), which provide an opportunity to perform the calibration only in digital form and thus avoid major drawbacks of digital-analog calibration are used. Also, the use of information redundancy in the form of redundant positioning system of notation makes it possible not only to simplify the calibration procedure and reduce the requirements for accuracy of digits , but also significantly improve the performance of converters.

Construction of self- calibrated ADC based - on RPCS has several advantages. First, it is possible to calibrate digits weights with significant deviations , which significantly reduces the requirements for a number of analog units of converters. The same factor allows, while using self-calibration procedures, to provide high metrological characteristics of converters in a wide range of temperatures and for a long operation time. Secondly, self-calibration can be applied practically all ADC of digit-wise coding.

Two main strategies of self-calibration are known . The first of these is called "bottom-up", the second one - "top-down". Algorithm "bottom-up" operates proceeding from the assumption that the lower order digit or a group of lower order digits are ideal. That is, the whole digit grid is divided into m "inaccurate" (higher order) digits, the absolute deviation of which may exaggerate half of the weight of lower "accurate" digit and (n-m) "accurate" (lower order) digits. It should be noted that the distribution into "accurate" and "inaccurate" digits is conditional. In a real converter, the relative deviations of "accurate" and "inaccurate" digits may be identical, but the impact of the errors of lower order digits is much more less than the influence of higher order digits. In the process of higher order digits calibration their weight is determined on the basis of lower order digits ("accurate "), that is why this strategy accumulates methodical quantization error. To reduce the latter during the calibration so-called additional digits , weights of which are smaller than the weight of the lowest order digit are used. The disadvantage of this approach is the extension of word length in the direction of lower-order digits.

The aim of this work is to improve the self-calibration algorithm for offsetting the quantization error.

To solve this problem we must:

– investigate the quantization error depending on the value of the auxiliary signal;
– propose a method of compensation quantization error;
– offer hardware implementation.

While calibration applying the strategy "bottom-up" [1, 3], the calibration of the weight of $i^{th}$ – digit $Q_i$ of ADC is twofold balancing of certain auxiliary signal, the first time using $Q_i$, and the second time without it. Then the code equivalent $K_i$ of calculated values of digit weight being calibrated, can be found by the formula:

$$K_i = \sum_{j=0}^{i-1} a_j{}' \cdot Q_j - \sum_{j=0}^{i-1} a_j{}'' \cdot Q_j, \tag{1}$$

where $a_j{}'$ and $a_j{}''$ – are, respectively, binary bits of codes of the results of the first and second transformations.

To eliminate these drawbacks, associated with accumulation of quantization error, the idea of multi- calibration is proposed. When applying this method one inaccurate digit is calibrated several times at different values of the auxiliary signal $A_{auxi}$. Minimum value of auxiliary signal $A_{aux\min}$. coincides with the value of digit weight being calibrated, and maximum value $A_{aux\max}$ – is defined as the sum of the weights of all low order digits. The value of A. if $a_i \in \{1;0\}$ is calculated by the formulas:

$$A_{aux\min i} = Q_i', \qquad i \in [l...n-1]; \tag{2}$$

$$A_{aux\max i} = \sum_{j=0}^{i-1} Q_j', \qquad i \in [l...n-1], \tag{3}$$

where $A_{aux\min i}$ and $A_{aux\max i}$ – are minimum and maximum values of the auxiliary signal for calibration of the $i^{th}$ digit ;

$Q_i' = Q_i + \Delta Q_i$, where $\Delta Q_i$ – is the deviation of the $i^{th}$ digit , $Q_i$ – is ideal value of the $i^{th}$ digit .

Operating value $A_{auxpi}$ of auxiliary signal must satisfy the condition $A_{aux\min i} \le A_{auxp_i} \le A_{aux\max i}$. Auxiliary signal $A_{aux}$ at the first and second calibration equals, correspondingly:

$$A_{aux} = K_l + \sum_{i=0}^{l-1} a_i{}' \cdot K_i + \Delta_{qu}{}', \tag{4}$$

$$A_{aux} = \sum_{i=0}^{l-1} a_i{}'' \cdot K_l + \Delta_{qu}{}'', \tag{5}$$

where – $\Delta'_{qu}$, $\Delta''_{qu}$ is quantization error, respectively ,at the first and second calibration.

On the basis of (4, 5) the quantization errors can be found by the formulas:

$$\Delta_{qu}{}' = A_{aux} - \sum_{i=0}^{l} a_i{}' \cdot K_i, \tag{6}$$

$$\Delta_{qu}{}'' = A_{aux} - \sum_{i=0}^{l-1} a_i{}'' \cdot K_i. \tag{7}$$

Graphical interpretation of the latter is shown in Fig. 1a, where MPA – is a unit of low order digit.

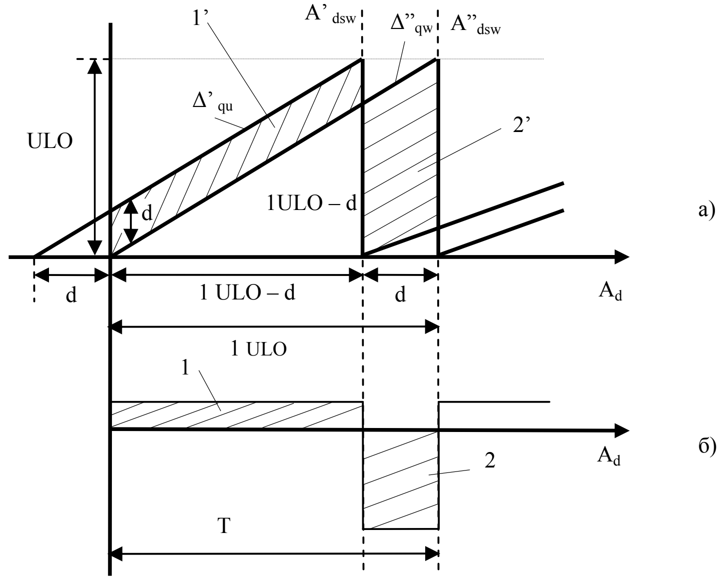


Fig. 1. Quantization error:
a) dependence of quantization error of the auxiliary signal Ad
b) resulting quantization error

In Fig.1a there are points at which quantization errors equal 0, these are the comparator switching points, and the value of Al in these points is determined by the expressions:

$$A_{adsw}' = \sum_{i=0}^{l} a_i' \cdot K_i, \tag{8}$$

$$A_{adsw}'' = \sum_{i=0}^{l} a_i'' \cdot K_i. \tag{9}$$

As a result of I-st and II-nd balancing the weight of the $l$-th digit can be calculated by the formula:

$$K_l = \sum_{i=0}^{l-1} a_i'' \cdot K_i - \sum_{i=0}^{l-1} a_i' \cdot K_i - \Delta_{qu}'' + \Delta_{qu}', \text{ or} \tag{10}$$

$$K_l = \sum_{i=0}^{l-1} K_i \cdot (a_i'' - a_i') - \Delta_{qu}'' + \Delta_{qu}'. \tag{11}$$

Therefore, the resulting quantization error is determined by the difference $\Delta'_{qu}$ and $\Delta''_{qu}$ shown in Figure 1b.

From Figure 1b it follows that the error of calibration takes both positive and negative values, and the dependence ($\Delta''_{qu} - \Delta'_{qu}$) is of periodic character, and the period of change T equals to the weight of low order digit. Hence, if you make several calibrations during one period T, and the result is averaged the formula:

$$K_l^* = \frac{\sum^{S} K_l}{S}, \tag{12}$$

where $l$ – is the iteration number, S – total number of iterations, then methodological error of calibration can be substantially reduced. And if we prove that the area of rectangles 1 and 2 in Fig. 1b are equal , then if $S \to \infty$ $K_l^* \to Q_l'$.

Since the areas of rectangles 1 and 2 in Fig. 1b equal to the areas of corresponding parallelograms 1 'and 2' in Fig. 1a, it is sufficient to prove that the areas of the latter are the same. Proceeding from the formula of parallelogram area calculation, we obtain $S_{parlg}1=d*(1-d)$, $S_{parlg}2=(1-d)*d$.

Simulation program was developed to prove the obtained results, the program is based on the above- mentioned algorithms and constraints. The result of the program operation can be seen in Figure 2.

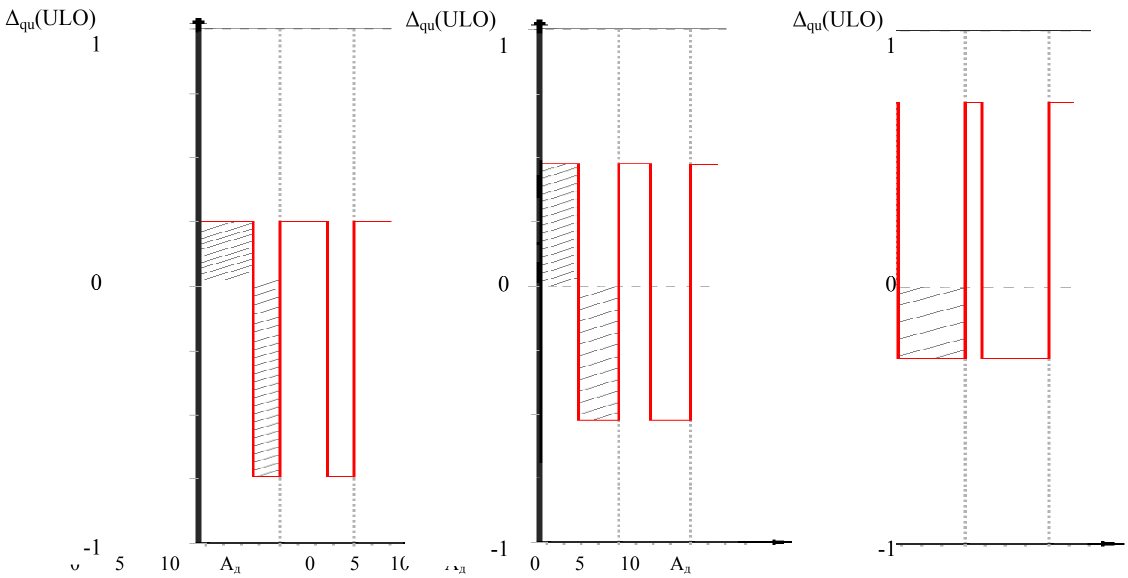


Fig. 2. The result of the program operation

On the base on the results obtained we can make a conclusion that the calibration procedure can be performed several times, changing the Ad within one low order digit at any interval of the range of auxiliary signal, and the resulting value is derived by averaging by the formula (12). We may avoid using additional digits, because the quantization error will be completely compensated.

The example of hardware implementation of the proposed idea based on self-calibrating ADC with digit redistribution on the basis of RPNS is shown in Fig. 3.

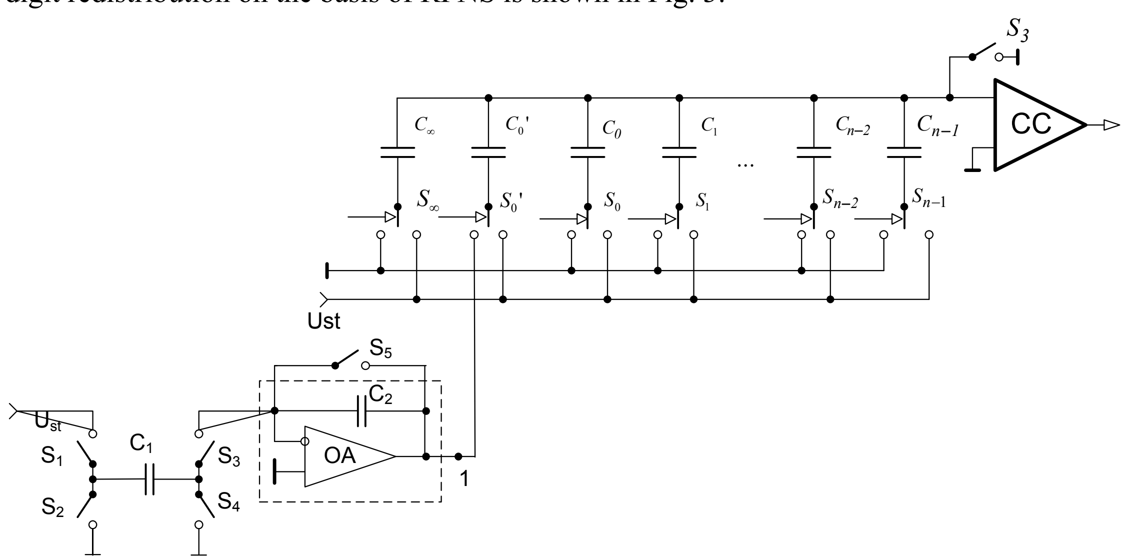


Fig. 3. Hardware implementation

While calibration of the $C_l^{th}$ digit in the first calibration we switch on $C_l$ and $C_k$ digits. The need of switching $C_k$ digit is due to the fact that zero shift t comparison circuit (CC) may be negative, thus to provide guaranteed connection of CC digit $C_k$.is switched on Then the result of calibration is the code equivalent of capacitances sum $C_l + C_k$ .Condition of $C_k$ selection criterion can be written by the formula:

$$U_{ref} \cdot \frac{C_l + C_k}{\sum_{i=0}^{n-1} C_i} > \frac{C_l}{\sum_{i=0}^{n-1} C_i} \cdot U_{ref} + U_{sh}, \tag{13}$$

where $U_{sh}$ voltage of zero shift of comparison circuit.

The auxiliary signal being formed can be represented as:

$$U_{ad_j} = U_{ref} \cdot \frac{C_l + C_k}{\sum_{i=0}^{n-1} C_i} + j \cdot U_{ref} \cdot \frac{C_1}{C_2} \cdot \frac{C_0}{\sum_{i=0}^{n-1} C_i}, \tag{14}$$

where $j \in [0,1,..., \frac{C_2}{C_1}]$. The ratio C1/C2 specifies the step of auxiliary signal change, forming necessary voltage.

Circuit operation starts from the selection of initial auxiliary signal $A_\partial$, for this purpose the key $S_3$ is closed and reference voltage $U_{ref}$. is supplied to capacitors Cl and Ck The remaining capacitors are connected to the ground. Then signal inversion occurs the key $S_3$ is open, capacitors $C_l$ and $C_k$ are connected to the ground, and the voltage generated is distributed to all capacitors of the matrix. At the next stage calibration procedure is performed, first time it is performed by switching on of $C_l$, and the second time -- without its switching on. Next balancing is carried out similarly, the difference is in voltage $U_{\partial nj}$, which is supplied in the point 1 and is defined by the expression (14), variable j specifies the number of balancing. Operation of auxiliary signal formation circuit is described in [1].When $j$ reaches the value of $C_2/C_1$, calibration is completed, and code equivalent to the weight of $l$-th digit is calculated by the formula (12).

## Conclusions

The article describes the methods of improvement the accuracy of the ADC and disadvantages of these methods. The method of digital self-calibration of A / D converter using weight redundancy is proposed, it allows significantly to reduce quantization error and avoid the usage of additional digits. The method is based on multi-calibration procedure performed at different values of auxiliary signal with further averaging of the result.

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***Zakharchenko Sergiy*** – Cand. Sc. (Eng), Assist. Professor, Department of Computer Engineering .

***Boiko Oleksandr*** – Master of Science (Eng), Department of Computer Engineering.
Vinnytsia National Technical University.