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BALANCING METHODS OF INTERMEDIATE STAGES OF PUSH- PULL DIRECT CURRENT AMPLIFIERS GAIN FACTORS

Some leading companies in the field of microelectronics, such as: Analog Device, ON Semiconductor, Intersil, etc. [1 - 4], manufacture push-pull DC amplifiers (DCA). The advantage of such devices is high linearity of transfer characteristic, high rate of operation as well as the symmetry of transient response to input bipolar pulse signal. However, in manufactured push-pull DCA there is a problem of establishing operating point of their intermediate stages. This feature prevents construction schemes of operational amplifiers with high overall gain factor.

Keywords*: direct current amplifier, balancing of gain factor.*

Actuality of the problem

It should be noted that the known push-pull balanced DCA, constructed both on field effect [4] and bipolar [1 – 3] transistors have a common drawback - low gain factor . Traditionally, this problem is solved by introduction of additional intermediate current reflectors and increase of the number of output stages. Nevertheless, this approach leads to decrease of the effective gain of the stage and increase consumption power of circuits. This greatly limits the range, and static characteristics of the circuits of push-pull DCA [1, 4]. The term "balanced" means equality of the transfer factors of the upper and lower channels of amplification, despite the fact that they are built on transistors of different types of conductivity having different current gain. However, the use of push-pull structures could potentially be promising for the construction of operational amplifiers provided the solution of the problem of provision of operation points of the intermediate amplifier stages. This would increase the gain, as well as maintain high linearity of the transfer characteristic and the symmetry of the transient response.

For solution of the problem the authors suggest two methods, the essence of which is:

a) transfer input push-pull stage in microcurrents mode [5, 6] with additional supply at the input of differential bias current, as well as replacement of the intermediate current reflectors by amplification stages with transfer factors at the level of β;

b) replacement of intermediate current reflectors by intermediate amplifier stages , operation point of which provide the application of compensation currents generated by means of double-circuit balanced reverse feedbacks on the basis of bi-directional current reflector (BCR) [7, 8].

Nevertheless, for these approaches, there is no solid scientific background, describing such methods. That is why the subject of the article devoted to solution of this problem is urgent. The purpose of research - analysis of methods of balancing of gain factors of intermediate amplifier stages of push-pull dc amplifier.

Objects of research:

1. Perform a review of the known schemes of push-pull DCA with symmetrical amplification channels.
2. Analyze the proposed methods of balancing of intermediate stages of push-pull DCA.
3. Obtain analytical expressions for small-signal transfer factors.

Problems solution.

Analysis of existing schemes of push-pull DCA produced by the leading companies in the field of microelectronics, in particular such as: Analog Device, ON Semiconductor, Intersil, etc. [1 - 4] demonstrates that these devices have similar four-staged structure. This can be illustrated by the model NCS2535 manufactured by ON Semiconductor [9]. However, the main drawback of such schemes, despite the increase in the number of stages, is low gain, which, moreover, depends on the load resistance. This problem is generated by non identity current transfer ratio for n-p-n and p-n-p transistors, as well as the use of serial structure of output stages, in particular those which use self-complementary push-pull circuit of composed Shiklai transistors .

However, giving up the use of current reflectors in the intermediate stages, having low current transfer ratio (at the level of ~ 1,0), and applying the methods suggested by the authors, it is possible to achieve significantly better results. So, let us analyze the operation of the circuit shown in Fig. 1, which implements the first method. Its essence is to transfer the input stage, which performs the function of the distributor of phase-divider (DPD) of the input current in micromode. In this case bias current ΔI_{bs} is supplied to the input of DPD. This allows to set transfer factors of DPD so that they were inversely proportional to β′ and β″, where β′ and β -are current gain of transistors Q′ and Q″ respectively.

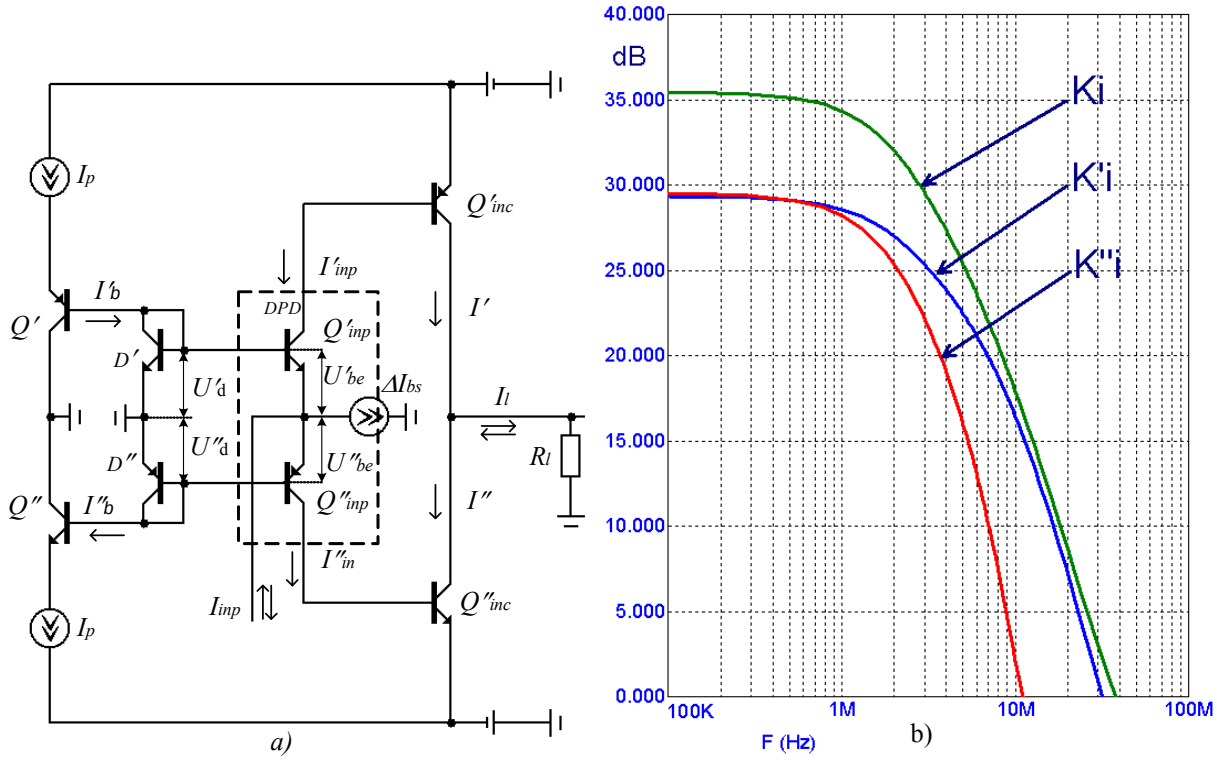

Fig. 1. Block- diagram of symmetrical push-pull DCA with input stage in the mode of microcurrents (a) and its AFC (b)

Here D′ and D″ are - transistors in diode connection , which set the operation points of DPD, and transistors Q′ and Q″ generate for them respective base currents:

$$I'_б = \frac{I_p}{B'}; \qquad I''_б = \frac{I_p}{B''},$$

where B′ and B″ are static amplification factors, respectively, of transistors Q′ and Q″, I_o –is current of operation point for nominal operation mode of Q′ and Q″.

We estimate the voltage on the diodes D′ and D″:

$$U'_д = \varphi_T \cdot \ln\left(\frac{I'_b}{I'_0}\right), \qquad U''_д = \varphi_T \cdot \ln\left(\frac{I''_b}{I''_0}\right),$$

where I'_0 and I″ are initial thermal currents [11], respectively T_1 and T_2,. Thus the total voltage of the diodes is defined as:

$$U'_д + U''_д = \varphi_T \cdot \ln\left(\frac{I'_б \cdot I''_б}{I'_0 \cdot I''_0}\right).$$

Assuming that I_{inp}=0 and I_{bs}=0, but I'_{inp}= I''_{inp}=I_{slc} (steady leakage current of operation point), we have

$$U'_{be} + U''_{be} = \varphi_T \cdot \ln\left(\frac{I_{slc} \cdot I_{slc}}{I'_0 \cdot I''_0}\right).$$

At the same time $U'_{\partial} + U''_{\partial} = U'_{be} + U''_{be}$, that is why, putting the right parts of corresponding equations we obtain :

$$\varphi_T \cdot \ln\left(\frac{I'_b \cdot I''_b}{I'_0 \cdot I''_0}\right) = \varphi_T \cdot \ln\left(\frac{I_{slc} \cdot I_{slc}}{I'_0 \cdot I''_0}\right).$$

After simplification we have:

$$I'_b \cdot I''_b = I^2_{slc}. \tag{1}$$

From (1) the following relation implies:

$$\frac{I'_b}{I_{нск}} = \frac{I_{нск}}{I''_b}, \quad :$$

If $I_{inp} \neq 0$ equality $|I_{нск}| = |I'_{inp}| = |I''_{inp}|$ is violated and we will have $|I'_{inp}| \neq |I''_{inp}|$, nevertheless the relation is performed:

$$I^2_{нск} = I'_{inp} \cdot I''_{inp}. \tag{2}$$

Then in accordance with the first Kirchhoff's law we obtain:

$$\begin{cases} I'_{inp} = I''_{inp} + \widetilde{I}_{inp}; \\ I''_{inp} = I'_{inp} - \widetilde{I}_{inp}, \end{cases} \tag{3}$$

where $\widetilde{I}_{inp} = I_{inp} + \Delta I_{bs}$ is total input current, I_{inp} – is the current from the generator of input information signal.

Substituting I'_{inp} and I''_{inp} in (2) we have:

$$\begin{cases} \left(I'_{inp}\right)^2 - \widetilde{I}_{inp} \cdot I'_{inp} - I^2_{slc} = 0; \\ \left(I''_{inp}\right)^2 + \widetilde{I}_{inp} \cdot I''_{inp} - I^2_{inp} = 0. \end{cases}$$

Finding the positive real roots of equations, we obtain:

$$\begin{cases} I'_{inp} = \frac{1}{2}\widetilde{I}_{inp} + \sqrt{\frac{\widetilde{I}^2_{inp}}{4} + I^2_{inp}}, \\ I''_{inp} = -\frac{1}{2}\widetilde{I}_{inp} + \sqrt{\frac{\widetilde{I}^2_{inp}}{4} + I^2_{inp}}. \end{cases}$$

Subtracting termwise from the first equation of the second one and define $\widetilde{I}_{inp}$:

$$\widetilde{I}_{inp} = I'_{inp} - I''_{inp}.$$

The condition of the balance of the circuit will be equal currents $I' = I''$. This is possible if $I'_{inp} = I'_b$, and $I''_{inp} = I''_b$, , therefore, it is necessary to satisfy the ratio $\widetilde{I}_{inp} = I'_b - I''_b$.

When $I_{inp} = 0$ we have $\widetilde{I}_{inp} = \Delta I_{bs} = I'_b - I''_b$. Thus, for the balance of the circuit is necessary to $\Delta I_{bs} = I'_b - I''_b$.

Let us analyze small signal transfer factors K_i' и K_i'', which in general terms are defined as:

$$\begin{cases} K_i' = k_i' \cdot \beta', \\ K_i'' = k_i'' \cdot \beta''. \end{cases}$$

For this we must additionally find transfer factors of DPD in the form:

$$k_i' = \frac{I_{inp}'}{I_{inp}} \text{ and. } k_i'' = \frac{I_{inp}''}{I_{inp}}.$$

This can be done analyzing the input resistances r'_{inp} and r''_{inp} of transistors Q'_{inp} and Q''_{inp}, determining the overall input resistance of the circuit, as shown in Fig. 2.

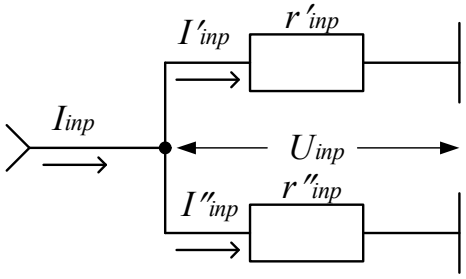

Fig. 2. The equivalent circuit of DPD input resistance

In this case the input voltage is defined in the form:

$$U_{inp} = I_{inp} \cdot r_{inp} = I_{inp} \cdot \left(r_{inp}' \parallel r_{inp}''\right). \tag{4}$$

However, r'_{inp} and r'' is set by relations:

$$r_{inp}' = \frac{\varphi_T}{i_b'} = \frac{\varphi_T \cdot \beta'}{I_o} \text{ and } r_{inp}'' = \frac{\varphi_T}{i_b''} = \frac{\varphi_T \cdot \beta''}{I_o}, \tag{5}$$

where β' and β'' -are differential current gains, respectively, of p-n-p and n-p-n transistors.

Substitute (5) in (4) and determine the equivalent input resistance:

$$r_{inp} = \frac{\frac{\varphi_T \cdot \beta'}{I_o} \cdot \frac{\varphi_T \cdot \beta''}{I_o}}{\frac{\varphi_T \cdot \beta'}{I_o} + \frac{\varphi_T \cdot \beta''}{I_o}} = \frac{\varphi_T \cdot \beta' \cdot \beta''}{I_o\left(\beta' + \beta''\right)}. \tag{6}$$

In this case the input voltage, taking into account (4) and (6) will be determined:

$$U_{inp} = I_{inp} \cdot r_{inp} = I_{inp} \cdot \frac{\varphi_T \cdot \beta' \cdot \beta''}{I_o\left(\beta' + \beta''\right)}.$$

However:

$$I'_{inp} = \frac{U_{inp}}{r_{inp}'} = I_{inp} \frac{\beta''}{\beta' + \beta''}, \quad I_{вх}'' = \frac{U_{вх}}{r_{вх}'} = I_{вх} \frac{\beta'}{\beta' + \beta''}.$$

Substituting I'_{inp} and I''_{inp} in output relations for K_i' and K_i'', we have:

$$k_i' = \frac{\beta''}{\beta' + \beta''}, \; k_i'' = \frac{\beta'}{\beta' + \beta''}.$$

Taking into consideration the values of k'_i and k''_i we obtain:

$$K_i' = k_i' \cdot \beta' = \frac{\beta'' \cdot \beta'}{\beta' + \beta''} \text{ and } K_i'' = k_i'' \cdot \beta'' = \frac{\beta'' \cdot \beta'}{\beta' + \beta''}..$$

Comparing K'_i and K''_i, we can conclude that they are symmetrical, ie equal to each other, namely:

$$K'_i = K''_i = \frac{\beta'' \cdot \beta'}{\beta' + \beta''} \ .$$

The total gain of the scheme will be determined in the form of:

$$K_i = K'_i + K''_i = 2\frac{\beta'' \cdot \beta'}{\beta' + \beta''}.$$

Fig. 1 b shows the graph of AFC of corresponding symmetrical push-pull DCA obtained by computer simulation, which proves the adequacy of the result obtained.

However, it should be noted that with increase of input signal frequency symmetry of transfer factors K'_i и K''_i becomes worse. In addition, the operation rate of the circuit decreases scheme since DPD operates in micromode.

To achieve greater operation rate and symmetry of intermediate transfer factors in the frequency range up to unity gain we will consider the second method of transfer factor balancing . It is based on DPD operation in nominal mode and to set operation points of the intermediate stages also uses compensation currents (CC). The basic scheme, which implements this method is shown in Fig. 3 a. To simplify the analysis we consider the circuit that does not contain the output stage. The values of compensation currents I'_c I''_c is constantly regulated by means of two-loop feedback, where bidirectional current reflector(BCR) is built-in. The given BCR is composed of two complementary connected current mirrors assembled on transistors, respectively, T_6 and T_{10}, T_7 and T_{11} respectively. Outputs of BCR across the first and second compensator current compensators (CC′, CC″) are connected to the inputs of intermediate amplifying stages, built on transistors T_9 and T_{12}.

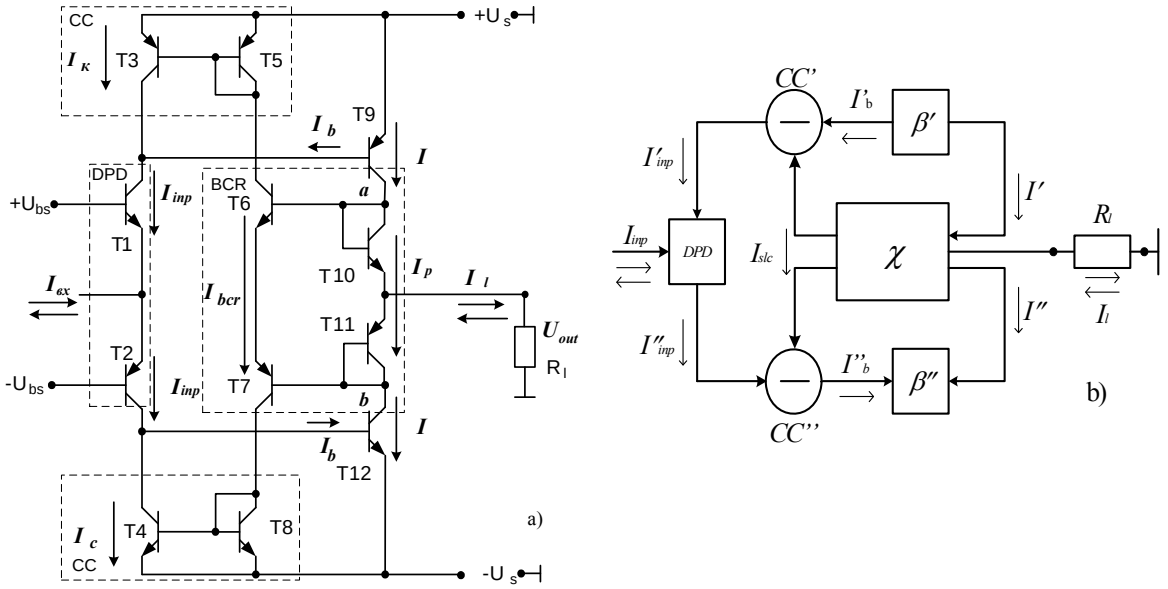

Fig. 3. Push-pull balanced DCA with BCR: a) simplified schematic diagram;
b) functional diagram

This approach allows to form constant component of operation current regardless of I′ and I″ changes . Proportional increments ΔI′ и ΔI″ practically do not influence the value of current I_{BCR}. Effects of feedbacks lead to balance relation maintaining in the circuit:

$$\frac{I'}{I_o} = \frac{I_o}{I''}. \qquad (7)$$

From the latter the equation follows:

$$I' \cdot I'' = I_o^2.$$

It is expedient to explain the analysis of the feedbacks impact on the basis of functional diagram shown in Fig. 3 b. However, if $I_{inp}=0$, then the input currents of DPD I'_{inp} and I''_{inp} are equal, and the output currents at the first moment of time are not equal. Voltage U_{ab}, which sets steady leakage current $I_{BCR,}$ is formed in points *a* and *b*. The latter, in its turn, sets I'_c and I''_c, which regulate base and corresponding collector currents I′ и I″ of transistors of intermediate stages. The circuit is balanced, when the equality I′ and I″ is formed.

If at the input of DPD circuit non-zero current I_{inp} will flow, then in base currents, T_9 and T_{12}, such variable increments gains will occur:

$$\begin{cases} i'_b = I'_{inp} \pm \Delta I_{bcr}; \\ i''_b = I''_{inp} \pm \Delta I_{bcr}, \end{cases}$$

where I'_{inp} and I*inp*″ is defined in the form [10]:

$$I'_{inp} = -\frac{1}{2} I_{inp} + \sqrt{\frac{I_{inp}^2}{4} + I_o^2}; \quad I''_{inp} = \frac{1}{2} I_{inp} + \sqrt{\frac{I_{inp}^2}{4} + I_o^2}.$$

In case of small-signal operation mode of amplifier , the inequality $I_{inp}<<I_o$ is performed so for evaluation of DPD transfer factor it is expedient to use the relation advisable to use the relation:

$$\begin{cases} k' \approx 0.5 \cdot \alpha''; \\ k'' \approx 0.5 \cdot \alpha'. \end{cases}$$

where - *k′* and *k″* are small signal DPD transfer factors, respectively, for the upper and lower amplification channels, and α′and α″ are transfer factors of circuits with a common base, 0.5 is transfer factorI_{inp} on collectors of transistors T1 and T2.

It should be pointed out that to estimate the intermediate transfer factors for the upper and lower channels of the intermediate stages of the circuit we must proceed from the theory of amplifying electronic circuits with feedbacks. [11]. It is known that the overall transfer factor in the circuit with the feedback can be determined in the form [12]:

$$K_{i\ ov} = \frac{I_{out}}{I_{inp}} = \frac{K}{1 + \chi K}, \tag{8}$$

where K is transfer factor for open loop feedback , χ is loop gain. It should be noted that if β′<β″ , then along the upper contour the positive feedback acts, and along the lower - negative, but if, then vice versa. Taking into account the actions of the contours of the positive and negative feedbacks for channels of symmetric DCA based on the relation (8) we have such transfer factors for intermediate stages:

$$K'_i = \frac{\beta'}{1+\eta} \text{ and } K''_i = \frac{\beta''}{1-\eta},$$

where $\eta = \chi K$ is loop gain .

Taking into consideration (7), in the zone of small signal we have $K'_i \approx K''_i$, therefore, comparing K′ and K″, we obtain:

$$\frac{\beta'}{1+\eta} = \frac{\beta''}{1-\eta},$$

where

$$\eta = \frac{\beta'' - \beta'}{\beta'' + \beta'}.$$

Thus, transfer ratios for the upper and lower channels of the intermediate stage will be defined by the relations:

$$K_i'' = \frac{\beta''}{1 + \alpha' \cdot \dfrac{\beta'' - \beta'}{\beta' + \beta''}}.$$

Note that regardless of the values of β′ and β″, which always significantly differ from each other [2], in small-signal zone we have the equality $K_i' \approx K_i''$. That is why in the circuit 2 there is the symmetry of transfer factors. Taking into account DPD transfer factors for the upper and lower channels, we have:

$$\begin{cases} \widetilde{K}_i' = K_i' \cdot k'; \\ \widetilde{K}_i'' = K_i'' \cdot k'', \end{cases} \tag{9}$$

Substituting in (6) the value of transfer factors for the upper and lower channels of push-pull DCA , and taking into account BCR feedback , we obtain the overall gain factor in the small-signal zone:

$$(K_i)_2 = \widetilde{K}_i' + \widetilde{K}_i'',$$

$$(K_i)_2 = \frac{1}{2} \cdot \left(\alpha'' \frac{\beta'}{1 + \alpha'' \cdot \dfrac{\beta' - \beta''}{\beta' + \beta''}} + \alpha' \frac{\beta''}{1 + \alpha' \cdot \dfrac{\beta'' - \beta'}{\beta' + \beta''}} \right).$$

Fig. 6 shows AFC, obtained by computer simulation for symmetrical push-pull DCA, which implements the II method. As it is seen from the graphs, the amplifier has the symmetry of the intermediate gain factor and practically the same frequency of single gain. The overall gain factor Ki is twice (6 dB) higher than the transfer factors of the upper and lower channels.

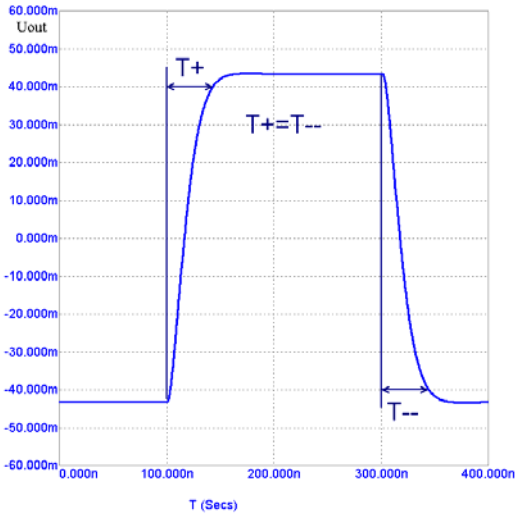

Fig. 3. AFC and transient characteristic of symmetrical push-pull DCA with bi-directional current reflector

For transient characteristic time constants can be defined in the form:

$$\begin{cases} \tau' = \dfrac{1}{2\pi f_{cp}'}, \\ \tau'' = \dfrac{1}{2\pi f_{cp}''}, \end{cases}$$

where f_c' и f_c'' – are cut-off frequencies into equal «–3 dB».

Since AFC graphs of intermediate channels are practically superimposed , ie. $f_c' \approx f^{"}_c$, that is why $\tau' = \tau''$, this means that the length of the front and rear edges of the transient characteristic are equal. Thus, given symmetrical push-pull DCA has the same transfer ratios for the upper and lower channels, and symmetrical transient characteristic.

Conclusions

1. The analysis of existing schemes with symmetric current transfer ratio is performed. Two methods aimed at provision of operation points of intermediate stages of DCA are suggested; they potentially allow to construct operational amplifiers with high transmission rates .
2. The suggested methods of balancing transfer factors of intermediate stages are analyzed. It is proved that these methods allow to maintain automatically nominal modes of operation points of the intermediate stages.
3. Analytical relations , which prove the ability to balance intermediate gains, despite the significant scattering of β′ and β″ values of n-p-n and p-n-p transistors, serving the basis for intermediate stages are obtained. It is proved that the transient characteristic of these amplifiers will be symmetrical when bipolar pulse signal is applied to the input .

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